

The semiconductor industry has developed almost exactly in the way that Moore's Law predicted it would. The Law's observation that the number of transistors on a given area of silicon would double every 18 months is reflected in the transitions to new process technology nodes. So 90nm begets 65nm and so on.

Until recently, this progression to smaller and smaller nodes was not affected by small scale problems. These problems, where they were encountered, tended to be more on the macroscale than the microscale. But as the industry moves towards 45nm and smaller technologies, what may have been small problems in the past are now turning into much larger obstacles. And the offending

How variability is affecting CMOS scaling. By **Graham Pitcher**.

articles are atoms.

Manufacturing variability has always held the potential for catastrophic and parametric yield failures. Traditionally, a conservative approach to design avoided these risks. However, at 45nm and below, the rules are so conservative that performance may be limited and die size increased – both opposite to the benefit of process shrinks.

David Desharnais, product marketing group director for Cadence's Encounter range, said: "If process variability is significant enough, it can result in the com-

plete loss of a chip. Being able to prevent that is one thing; not getting the performance you expect is another. Variability is a killer and that's why Cadence is putting variation awareness in the hands of designers."

In the latest version of its Encounter tool suite, Cadence says it is 'going beyond rules' to model directly critical elements of the manufacturing process – lithography, chemical mechanical planarisation and random variation. In other words, says Cadence, 'what you design is what you get'.

Mentor Graphics has also been active in this area, unveiling Calibre LFD – for litho friendly design – early in 2006. The move was, it claimed, 'a major rethink of the IC design creation flow', which

Roughing things up





addressed the 'urgent issue' of how to manage process variability in the early stages of design creation.

"In the past, it has been the foundry's responsibility to ensure printability," said Joe Sawicki, general manager of Mentor's design to silicon division. "With Calibre LFD, designers can have a big impact on how well designs yield through the variances of the process window."

Asen Asenov is professor of device modelling at Glasgow University, where he is also leader of the Glasgow Device Modelling Group and academic director of the Glasgow Process and Device Simulation Centre. As such, he is looking to develop tools which can model advanced semiconductors. Part of that work requires him to understand the problems which advanced processes bring.

"Variability is one of our major research themes," he said. "We started to simulate variability about 10 years ago. Since then, I've been a 'bad messenger', telling people about the problem."

This problem, he says, is present at the 90 and 65nm nodes. "At 45nm, it's very serious; at 32nm, the problem will change the way in which circuits are designed."

And he says some devices are already facing problems, such as sram at 45nm. "If you make sram at 45nm in the same way as you make it at 90nm, then it won't work. People have design rules to make 45nm work, including redundancy, but it's the first serious design challenge posed by variability and it's unavoidable."

There are a number of variability factors. "Process variability has been known about for years," said Prof Asenov, "and there is some ability to control dimensions. Focusing problems with lithography can also cause problems, creating features that are slightly larger or slightly smaller; in turn, altering transistor characteristics." Prof Asenov added this can vary not only across a wafer, but also from wafer to wafer.

"These effects can be controlled with good equipment and well trained engineers. But, whilst you can tune variability, improve uniformity and get a better yield at larger dimensions, variability becomes more difficult to control at smaller dimensions."

Another effect is optical proximity compensation. "Depending upon how you do this," Prof Asenov contended, "you get different shapes from transistor to transistor. This is variability, but it is predictable. DFM can cope with this and eda vendors factor this into their circuit simulation tools."

But another kind of variability, says Prof Asenov, is unpredictable. "Devices are so small that variations in atomic structure and dopant levels bring big variations in device characteristics."

He used dopant levels as an example. "Dopant atoms end up in different places. Maybe there is the same amount of dopant, but it's distributed randomly and one transistor may have more than another. Because the transistors are so small, the number of dopant atoms is only around 100. So one transistor may have 90 dopant atoms, whilst another may have 110. Both will behave in a different way."

And, as dimensions continue to shrink, the number of dopant atoms will reduce and the statistical variation gets bigger.

And there's line edge roughness. "Photoresist molecules are large; around 2nm," Prof Asenov noted, "so line edge roughness can be up to 5nm. This is difficult to reduce unless you use photoresists with smaller molecules. There's a significant variation, even with perfect lithography."

One way to overcome at least some of the problems is to move away from the traditional bulk mosfet in favour of thin body devices. "If you move to thin body mosfets," he continued, "you don't need dopants in the region. Take away the doping and you remove the variability associated with the process. That's why memory manufacturers are moving to thin fet transistors to reduce variability and to improve sram design."

In the end, he believes, variability is here to stay and the only way to deal with it is to factor it into designs. "That's what our project is all about," he enthused. "We assume there's variability we can't control, so what can we do at the design stage to cope with it?"

Whatever solutions Prof Asenov's

group comes up with, they will be computationally challenging. "We will have to replace traditional design approaches because you don't know where the 'corners' are. The only way to do it is to simulate statistically using a range of transistors. This is very demanding and



"At 32nm, the problem will change the way in which circuits are designed."

Prof Asen Asenov, Glasgow University

designers are already having problems with complexity."

One possible solution is to hide simulation and verification complexity from the designer. "They will see a traditional workflow, but we'll use algorithms running on grid technology – hundreds of processors – to handle statistical verification and simulation," he concluded. ☺

The National Microelectronics Institute, in collaboration with the UK's nanoCMOS project, is staging Europe's first international conference dedicated to cmos variability. The conference, on 23 October in London, will bring together companies representing the semiconductor supply chain and major research initiatives in order to analyse the implications of variability on semiconductor design.

For more information, go to:
www.nmi.org.uk/events/DFM_23102007.htm