



Mighty multicore

In the past, more computing power was squeezed from a chip simply by turning up the clock rate. But physical limits have imposed themselves on that approach. A combination of heat generated and power consumed meant it was the end of the road for the single chip processor – at least at the top of the range.

The solution was multicore processors and devices from companies such as Intel and AMD have already found their way to market in the latest pcs.

But multicore processing is also appearing in the SoC world and the first instances of this came a couple of years ago. In particular, ARM launched the ARM11 MPCore, which could be configured with up to four processors and a total processing power of 2600 Dhrystone MIPS.

Now ARM has launched another configurable multicore processor; this time, adding the device to its Cortex range. Cortex is a family of processors providing a

ARM's latest multicore processor brings muscle to high performance designs. By **Graham Pitcher**.

range of solutions targeted at particular applications. The M series comprises devices for deeply embedded designs, whilst the R series offers embedded processors for real time applications. But it's the A series that will be the home for ARM's latest multicore processor. A, in this instance is for application and the Cortex-A9 MPCore is designed for performance.

However, recognising that not every user will need multicore levels of performance, a single core variant is also available – the Cortex-A9.

The reason for multicore is outlined by John Goodacre, ARM's multiprocessor programme manager. "Multicore means

we can offer increased performance without increasing power consumption."

And the move by ARM reflects growing need for more computing power in the consumer electronics sector. "The embedded market has been seeing a lot of convergence; some of which has been going on for some time," Goodacre noted. He gave the example of the set top box. "An stb now needs multiple video channels, with Java for example. A single core device can get to about 2000Dhrystone MIPS, but efficiency breaks down if you go beyond that. The MPCore can take that performance level up."

One of the drivers for providing a core with the processing power of the A9 MPCore is demand from a broad range of market sectors for the same thing. Goodacre explained: "There's a range of markets which have common needs, such as increased power efficiency with higher performance, as well as the ability to share



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John Goodacre, ARM

software across multiple platforms. By providing a road map for Cortex, we can take users to where they want to get."

The A9 MPCore is targeted at high performance handsets, as well as networking products and automotive infotainment. "And automotive people," Goodacre continued, "are putting real time applications onto this core."

The A9 single core, meanwhile, is aimed at mass markets where, in his view, customers can 'take it, plug it in and make

the product go better than before'. "It brings more performance for less power to ARM11 type users," he added.

STMicroelectronics, one of the Cortex-A9 licensees, plans to use the core in personal multimedia products. According to Jyrki Hannikainen, general manager of ST's Application Processor Division: "The next wave of mobile phones and portable multimedia devices will ... demand superior processing power to manage media such as web content, mobile games, video on the go, map services and digital still camera class imaging. By combining the Cortex-A9 processor with ST's mobile multimedia platform, ST will continue to deliver high performance and low power chipsets and platforms."

A9 MPCore brings a range of companion products, such as L2 cache controllers and a media processing engine, blending a floating point unit (fpu) with the NEON advanced SIMD unit introduced with the Cortex-A8. The reason for this spread of functionality, said Goodacre, is that much of the embedded systems market is now looking for something application specific. "You might want to include an fpu inside a printer, for example. The high performance fpu can be used to enable a 1200dpi printer capable of 24bit colour."

"What we've announced," said Goodacre, "is the first synthesisable processor capable of delivering 8000DMIPS, compared with the Cortex-A8 which only produces 2000DMIPS."

Equally important, in Goodacre's opinion, is the combination of multicore abilities with the Cortex architecture.

Achieving the levels of performance which ARM claims for the A9 MPCore has required what the company calls 'key microarchitectural advances'. With a dynamic length, eight stage superscalar, multi issue pipeline featuring speculative out of order execution, the A9 MPCore can execute up to four instructions per cycle in devices clocked at more than 1GHz. Common instructions are said to take nine cycles, whilst more complex ones will take 'less than 11'.

There's also the ability to use out of order instruction despatch and completion. This allows up to four instructions to be sent and seven instructions completed per clock cycle.

"There's a lot of new technology compared to the A8," Goodacre contended. "Some of this was introduced with the ARM11, but has been enhanced."

The A9 MPCore can be configured to include from one to four cores. "And the technology is all about working those cores together efficiently," Goodacre continued. "In terms of the hardware, the core has been optimised so that it can handle synchronous and asynchronous processing."

Making sure the cores work together efficiently is the Snoop Control Unit, described as a high speed interface to move data between caches, as well as distributing interrupts.

"It's all well and good having a great processor core," Goodacre admitted, "but if it doesn't allow the system to operate well, then it's not that good. So the MPCore has technology that enables a better interface with an SoC, bringing the power and performance advantages of the MPCore to other system components."


That technology is the Accelerator Coherence Port (ACP), which allows DMA and crypto engines to access the cache hierarchy. "Until this," Goodacre concluded, "programmers would have to flush the cache before talking to an accelerator, with power and performance penalties. Now, the system can signal to an accelerator that there's something to do without having to use interrupts." 

Figure 1: Cortex-A9 MPCore processor structure

