



All change please!

Change is a constant and nowhere does this apply more than in the electronics sector. That change means electronic design is a much different discipline than it was a decade ago.

What technology trends have had the most impact on organisations? Plextek's managing director Colin Smithers highlights two issues from a system level perspective. "Design tools have improved and broadened in their scope. This is changing the way people work, from the cad design flow to the end result. It has resulted in a requirement for learning: of the tools themselves and the implications of their use." The second issue is thermal design. "As device sizes decrease, getting heat out of them is becoming an issue for everybody." Power consumption is a related issue. "This was traditionally a problem only because it generated heat. Now, it is an issue that leaves no design untouched," he observed.

From an academic perspective, Tony Harker, ceo of the Institute for System Level Integration (iSLI), says: "The main trends are the march towards complex verification of large digital systems, mixed mode design in the analogue and digital domains, concurrent hardware and software development and, of course, the move to multi cpu systems. All of these have meant that iSLI's material has required constant appraisal against industry trends.

"The vital QA mechanism within UK universities means the academic world may not be able to respond quickly enough to match industry's tack. iSLI's way of addressing this is through targeted

The last decade has seen profound changes in the way design engineers work.

What does the future hold?

By Vanessa Knivett.

Continuing Professional Development in key areas."

Echoing some of Harker's thoughts, Philippe Magarshack, vice president of STMicroelectronics' technology R&D group, pictured below, provides a chip level perspective. "Many changes have been driven by Moore's Law," he believes. "It has demanded new process technologies, where deep sub micron effects are being encountered. This has created the new discipline of Design for Manufacture, which translates into new tools to quantify the

impact of litho, more process steps or tools to simulate electrical variability induced by those effects."

Other consequences of design complexity he cites include an 'explosion in demand for functional verification' and multiple processors per chip, each with its set of annotated software and drivers. This has created a need for codevelopment of the software and the SoC. "Some product development divisions within ST now have more software engineers than hardware engineers and sometimes the annotated software is the critical path, rather than silicon."

At a practical level, Magarshack mentions a move from simply managing static/leakage power to dynamic power, the emergence of high speed serial links or interfaces such as DDR2 or DDR3, and 'more cumbersome timing sign off', with perhaps 40 to 50 timing corners per design.

"One consequence of design complexity," he continues, "is an important switch in the level of abstraction at which we describe SoCs. Ten years ago, we worked at the rtl level, then it was Verilog. Now, in most cases, we are at a higher level, using System C transaction level modelling. This has boosted productivity by three to four times." In addition, he notes the trend towards system level solutions, thanks to the adoption of high level synthesis. "Many IP designers can design their digital IP in C or System C and use guided high level synthesis to create the rtl and, eventually, the final design."

Harker agrees that IP is now key to the typical ic design flow. "Concurrent design and the use of





predesigned IP is vital in today's design flow – both in software and hardware. We have heard a lot about IP over the past decade. A lot of engineers were actively hostile to the thought of using someone else's blocks, but the days of 'Not Invented Here' are definitely over. System designs, both on and off chip, simply could not be achieved without predesigned IP. Only by using such IP is it possible to start designing software early enough to match the hardware development phases."

So what impact has this change had on

broader engineering pedigree."

Magarshack's ic design view? "My recommendation to students is to gain a detailed understanding of how 65nm or 45nm transistors behave. This will help them understand low power features, such as biasing or retention, and the causes of performance variability. Even if you are designing at an architecture or rtl level, you need this level of understanding."

It seems iSLI is on the case. Says Harker: "The march towards ever smaller geometries means silicon designers need to be masters of many different trades. The previously disregarded effects now seen in deep sub micron silicon mean design engineers also need to have a working understanding of device physics, mechanics, emi, reliability and other aspects. All of this means that institutions such as iSLI need to produce engineers that are adaptable and have a good grasp of fundamental issues, such as analytical techniques and structured problem solving."

Crystal ball anyone?

Smithers sees further pressures on time to market. "It's the rate at which things get to market and to volume. We don't have the luxury of testing things on small markets and things get scaled very quickly."

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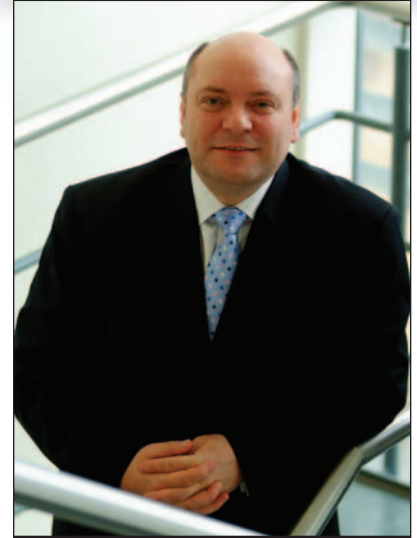
Colin Smithers, Plextek

skills? Says Smithers: "Living in a purely hardware or software world is, perhaps, more dangerous now than it once was. For example, you can't ignore layout and high frequency effects and there is emc and radiation. Hence, designers should be multidisciplinary, although many are not."

It's the same in the academic world, as Harker explains. "The days of niche designers is disappearing and our technical staff need to have a much

Magarshack thinks future process moves pose quite a few challenges, but he hopes the eda industry can help. "Process variability process was an issue at 45nm. We are now starting to work on 35nm and are working actively with the eda industry to do systematic variability modelling to better understand lithography and chemical mechanical polishing effects.

"Secondly, random variability between transistors requires statistical analysis.



Harker: "We run the risk of removing a degree of designer freedom in pushing the limits of technology."

We have heard about this for many years, but it is still not useable."

He hopes that design rules – which change from one process to another – can be standardised; that tools that enable the codesign of digital, analogue and rf become available; and that IP gets smarter, answering questions about itself such as 'how many cycle times are needed for this or that?'

Harker agrees that more design automation is needed, but questions its impact on designer freedom. "As we move silicon inevitably to a smaller number of foundry processes (due the net inherent cost of production), we run the risk of removing a degree of designer freedom in pushing the limits of technology. In doing this, we also remove the option to differentiate products in the marketplace. This will inevitably produce complex 'vanilla' products that differentiate using application software.

"Whilst this in itself is not a bad thing, I worry that it will stifle creativity within the hardware designers' world. We need to work hard to maintain core skills that allow engineers to question the norm and innovate as appropriate." ■