



Beyond the boundary

Boundary scan, as defined by IEEE1149.1, has proved invaluable for device programming and board level manufacturing test applications. However, some envision that its potential lies far beyond this, to connectivity testing, diagnostics and device programming at a system level.

Whilst using boundary scan chains to add system level capabilities isn't new,

SJTAG is not yet a standard, but there's a compelling case for it to become one.

By Vanessa Knivett.

there are some challenges to doing so. Designers can and do devise solutions for

implementing system level boundary scan, but there's no compatibility between solutions. One group hopes to change that.

The system level boundary scan (SJTAG) initiative began in 2005, aiming to extend the test and configuration capabilities of IEEE1149.1 to complex multiboard systems. The group's mission is to standardise the processes and methodologies for SJTAG applications in a bid to make them vendor independent and non proprietary.

Chaired by Dr Ben Bennetts, the group has representatives from ASSET InterTech, BAE Systems, Ericsson, Firecon, Goepel Electronics, JTAG Technologies, Lucent, Motorola and Selex Galileo among its members.

Touching on some of the challenges faced by those attempting to implement system level JTAG at present, Ian McIntosh from Selex Galileo explains: "We are trying to put in place some guidelines that enable people to create system and subsystem designs that you can test on whichever test platform you have available at that particular point, whether it's board level or system level, without having to reengineer the test applications and without imposing constraints that you have to use specific components."

Representing the end user group, McIntosh is keen for an open standard that is independent from both device and software tool vendors. He believes it is key that SJTAG is not too prescriptive. "I think of SJTAG as an enabling technology and it's up to you what you want to do with it. Users should be able to cherry pick applications to suit their particular needs, but having put basic infrastructure in, know that everything is available to them."





The design in case

Why should a designer consider SJTAG compatibility? With full life issues of concern in a number of markets, proponents envisage that SJTAG could enhance reliability at a system level and potentially reduce operating and maintenance costs once a system is in the field.

Speaking from Selex Galileo's



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perspective, MacIntosh says: "If we need to do a firmware update, to reprogram the fpgas in a system to cope with a new version of software, the implications of being able to use a laptop to connect to a Jtag port and do the reprogramming – with the system's cover on and in situ – would be immense for us and for our customers. We wouldn't need expensive field service test sites at every repair depot, because we could do detailed diagnostics without even opening the box."

Whilst the catalysts for SJTAG were manufacturing oriented structural test and device programming, new applications are in discussion. Hence, the SJTAG group has developed a set of 10 use case scenarios that describe how boundary scan could be used at a system level (for more, see www.sjtag.org). These include SJTAG for software debug; failure analysis; and for device

programming for built in self test.

Explaining how SJTAG could be used for software debug, MacIntosh explains: "In the case of a software failure, SJTAG would enable you to create a map of what state the hardware was in when the error occurred and what the software did ... potentially giving you access to things that would be invisible to software debugging tools. You could also turn that capability on its head and use boundary scan to inject faults."

Extending Jtag

One of the tasks for the SJTAG group is to make the concept more software friendly. MacIntosh explains: "We need to limit the amount of permutations you can have to get it into a kind of state where software tooling can deal with it predictably. At the moment, some of the tools fail to cope with some of the topologies that are in use and the level of capability of these tools varies as you move across different

vendors – some work with some topologies and not with others."

Providing a tool vendor's perspective, Heiko Ehrenberg of Goepel Electronics comments: "Today's scan chain management devices implement proprietary protocols to switch chains, which means tools need to support these different protocols to enable system level JTAG applications."

"Tool development effort can be high. As boundary scan connectivity tests are developed, based on board netlists that are merged together for a system level test, the system configuration is fixed for a specific test program. If the system configuration changes – maybe because boards and modules can be located in different system slots, or because boards contain different components or sub modules – such connectivity tests need to be generated for all possible

configurations during test development.

"Alternatively, tests need to be generated and compiled at run time, based on the system configuration. The latter requires information about the specific system configuration. This is currently not available in a standardised format, making it very difficult for tools to be flexible enough to support such system variations."

Ehrenberg adds: "An SJTAG standard has the potential to eliminate these problems by defining a standard description language for board and system features related to test. There will be effort in implementing features required for a tool to be SJTAG compliant, but the long term benefits should outweigh those efforts."

As SJTAG is based on the principles of IEEE1149.1, it would make use of the conventional five wire TAP interface, plus a switching mechanism. But there is much yet to be defined. One discussion point is whether SJTAG should support a star configuration or/and a multidrop architecture (the latter would support multiple boards with the same state machine in JTAG).

Language definition

Meanwhile, the SJTAG group is about to start work on the language definition and is investigating an object oriented structure. Notes MacIntosh: "At moment, we have a BSDL file that describes how a device works from the JTAG point of view. The task is to extend this to board, then system, level issues." Whilst the group is considering existing language standards, such as SVF and STAPL++, there are some challenges with these.

The group is due to submit a project authorisation request to the IEEE by the end of 2008, after which SJTAG could be recognised as a draft standard.

MacIntosh concludes: "We wanted to be sure we had fully understood the problems before submitting the proposal. If you look back to the IEEE49.5 maintenance bus – which only lasted a few years – there wasn't a complete understanding of what people really needed." ■