



# Multicore magic

*Multicore processor aimed at heart of comms web. By Roy Rubenstein.*

**F**reescale's recent decision to sell its wireless chipset arm and bolster its remaining businesses through acquisitions has been backed with action (See NE, October 14, p10). In October, the company acquired Intoto, a security software specialist for datacom networking equipment.

Historically, firms such as Freescale provided the chips and customers developed the software. As processors have become more complex, some of Freescale's competitors have started to deliver a complete set of software with their processor. "The Intoto acquisition will enable Freescale to build its own software competency," said Linley Gwennap, principal analyst at The Linley Group. In particular, it will enable the firm to deliver more software with its latest QorIQ (pronounced 'core IQ') networking processor family.

Freescale is the leading supplier of processors for networking and communications, according to the Linley Group. Its devices have always been popular for control plane applications, overseeing and managing systems. With

QorIQ, the company can now play in control plane and packet processing intensive 'data plane' applications. Freescale can also compete with the specialist asic designs favoured by large telecom players and with network processor vendors such as Cavium and RMI.

QorIQ, the successor to Freescale's PowerQUICC, signifies the company's embrace of multicore processing. PowerQUICC already has dual core devices, but the first QorIQ devices include the P4080 based on eight e500 Power Architecture cores.

### Radical requirement

"[Processing] performance is increasing for all sorts of applications," said Piotr Weglicki, Freescale's systems marketing and applications director, networking and multimedia group. Wireless broadband, for example, requires a tripling in processing performance each year, rather than the doubling every 18 months that device scaling traditionally brings. He says: "You will not solve such a radical requirement using traditional methods; new processing approaches are required."

To this end, Freescale is going from 90nm to 45nm, bringing a higher processor clock speed and acceptable power consumption.

"This was an important decision because it will greatly improve size reduction and power efficiency," said Eric Heikkila, director embedded hardware and systems at VDC Research Group.

QorIQ comprises five platform families, with different price/performance targets achieved by varying the number of cores, on chip peripherals and clock speeds.

Of QorIQ's five platforms, three have been detailed. The P1 and P2 platforms comprise four announced pin compatible devices. The P1010 and P1011 will be single core devices, while the P1020 uses two e500s clocked at up to 800MHz. The P2 family's first devices will comprise the single core P2010 and the dual core P2020, clocked at up to 1.2GHz. The P1 and P2 devices are aimed at cost conscious applications, such as network attached storage and media gateways.

The first high end P4 device, the P4080, can be clocked at 1.5GHz while consuming less than 30W. It is targeted at

Illustration: Oliver Bursten/DebitArt



applications such as radio network controllers and edge routers for metropolitan networks.

QorIQ devices are based on the 32bit e500 Power Architecture core, also used for PowerQUICC devices. This provides software continuity and reflects Freescale's decision to focus on scaling processing performance by going parallel, rather than concentrating on enhancing the individual core's design.

The P4080 uses a three level cache hierarchy to ensure the eight cores are not idly waiting for data. Each core has its own 32kbyte Layer 1 instruction cache and 32kbyte data cache, as well as a private 128kbyte Layer 2 cache. All eight cores share two 1024kbyte Layer 3 caches, which store common data structures. Cache memory can be used flexibly: data can be locked in the cache if it is always needed, and can bypass the cache if it is used only once.

The P4080 uses a non blocking switch fabric, dubbed CoreNet, to connect the cores and the cores with on chip hardware and the I/O interfaces. The device's also have hardware blocks – application accelerators – that implement security, pattern recognition and the packet processing tasks of queuing and buffering. The I/O includes eight 1Gbit and two 10Gbit Ethernet ports, two RapidIO and three PCI Express interfaces supervised by two frame managers. The frame managers also oversee the buffering and queuing hardware.

The P4080 supports virtualisation, used to partition resources. The virtualisation concept separates software functions from the underlying hardware to improve utilisation. Embedded hypervisor software, a slim piece of code, is loaded onto the device when first powered. Hypervisor enables the processor to run more than one operating system on the device – even on the same core.

"Hypervisor loads the operating system partitions and then runs them," said John Logan, a Freescale senior applications engineer. For example, Linux can be used for the applications, a second operating system for control plane tasks while a third real time operating system will oversee the

high speed, low latency data flows.

Freescale has teamed with several software partners, including ENEA, Green Hills, MontaVista, QNX, Virtutech and Wind River, to help customers address multicore software issues. "The [software] ecosystem that Freescale has built will be very important, especially as the roadmap progresses to eight or more cores," said Heikkila.

Working with Virtutech, Freescale has developed a hybrid simulation environment. This includes Virtutech's Simic functional simulator and an in house cycle accurate simulator. Simic can run a design that includes the applications, the operating systems and even complete

QorIQ devices will help developers program the more complex QorIQ designs with familiar tools. This contrasts with tools designed solely for multicore npus.

Freescale has yet to detail its P3 and P5 QorIQ devices, although these will likely use more than two cores. The platforms scale linearly with processing performance such that the P5 will tackle the most demanding applications at the expense of power consumption.

Freescale has also said the CoreNet switch can support more than 32 cores and several core types. Thus, future devices will likely include other Power Architecture members along with dsp cores. "We've got the technical

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software stacks. It can also be used to simulate a core on a QorIQ device to complete multitracked QorIQ based systems connected via a wide area network.

Engineers can begin developing applications before they get silicon and then use the tools to optimise the software once they have target hardware. "Companies are already using the Virtutech simulator [for QorIQ designs]," said Weglicki.

Having the same development environment shared across lower end single and dual core, as well as multicore,

capabilities, but future devices will be dictated by the market," said Weglicki.

Gwennap expects Freescale to further enhance the e500 architecture for customers who want greater processing performance, yet who are reluctant to port their designs to a multicore device.

"There are a lot of companies that have software on one cpu today and are concerned it will take too much work to run [the code] on multiple cpus," he said.

According to Freescale, P2 devices will sample in Q1 2009, P4 will follow in Q3 2009 and P1 in Q1 2010. ■

