Facing the *challenge*

Testing times for fpga specifiers. By ***Chris Shaw****.*

Embedded instrumentation throws up all manner of challenges for the humble designer. As technology becomes ever more complex, the need for external instruments such as oscilloscopes and logic analysers increases proportionately. The problem is actually using them.

Today, the sheer density and integration of semiconductor devices on boards has escalated to the point that any inadequacies of external and modular instrumentation have become immediately apparent. Glenn Woppman, president and ceo, Asset InterTech, explained: "Embedded instruments can take many shapes and forms. Soon the capabilities of an oscilloscope will be embedded as an additional resource on a chip. The types of instruments that will be embedded will be determined by many factors, such as the needs of the application, the resources of the system and the ingenuity of the chip's design."

FPGAs with embedded test functionality allow designers to automate, access and analyse instruments at the chip level and can be called upon during every phase of a system's life cycle. Woppman continued: "For example, design validation has a critical need for the capabilities of embedded instrumentation. Without it, the design team cannot test and validate the signal integrity of high speed busses. As the circuit board, sub assembly or system move into manufacturing, embedded instrumentation will be used to perform at speed tests and diagnose failures. And, once the product has been deployed in the field, embedded instrumentation could be accessed and engaged locally or remotely by service technicians to diagnose performance issues and troubleshoot failures."

The fast paced consumer market is forcing engineers to cut design times and add more features, while cutting power and costs. As a result fpgas with short design cycles and easy design iterations, are taking on more of the system complexity and control. The design flow for fpgas continues to evolve as the content of the fpga grows from basic glue logic to system master in many applications.

This is especially true when using an embedded processor inside the fpga, as Actel's principal engineer Wendy Lockhart explained. "In order to reduce design time, it is critical to be able to begin

board manufacturing early and trust that you can figure out the contents of your fpga in parallel. The ability to program your fpga in system, perform system testing and reprogram the device as needed can significantly improve your time to market and competitive edge. When testing a system with the fpga on board you will need access not only to the pins of the fpga, but to the signals within the fpga due to the increased size and complexity of modern fpga designs."

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Actel has solution in the shape of its Igloo, Proasic3 and mixed signal fusion fpgas. "At the highest level, the test flow involves embedding a test block in the rtl before synthesis," continued Lockhart. "The design is then compiled and programmed into the fpga on the board and then test and debug can be performed using the programmer connection, with results viewed on the computer. When the development stage of the design is completed the test block can be removed from the design if desired and the reduction in size may allow the use of a cheaper part for high volume production. To facilitate this last step Actel provides pin compatible device migration within each family for many packages."

Designers face a number of problems when addressing the low cost fpga market. Low performance and lack of features are key complaints. Nevertheless, both can be addressed by looking at the key performance bottlenecks in a system which tend to centre around high speed I/O protocols and abundant embedded memory.

Low cost fpgas

According to Lattice Semiconductor's director of marketing for high performance solutions Shakeel Peera, it's possible to architect a low cost fpga fabric while 'hardening' the required I/O, memory and dsp blocks that are required in high performance systems. This approach, he says, will preserve the low cost nature of these fpgas, while delivering the needed system performance requirements. "Timing closure is still one of the key problems that face fpga designers today," he remarked. "careful floorplanning and the need for fpga vendors to support robust floor planning tools becomes key. Intelligent, architecture aware synthesis tools also require the fpga vendor to work very closely with third party synthesis vendors during the early stages of defining fpga platforms. As high speed I/Os and serial protocols become permanent fixtures in fpga designs, designers worry about ensuring that the signal integrity of their fpga I/O and serdes will hold up in their specific environment, taking into account other devices that need to interoperate with the fpga. For this, high speed I/O models, switching noise calculators need to be provided."

When the need is for critical measurement functions, without embedded fpgas, it is not always possible to achieve as Glenn Woppman commented: "There is no denying the fact that the momentum behind embedded instrumentation has gotten a big push from necessity. But, on the positive side, there are just as many benefits that are pulling chip and system suppliers toward embedded instrumentation. One of these is the life cycle efficiency benefits that accrue to embedded instruments starting in chip design and extending all the way into field repair in deployed systems."

Benefits

The benefit of fpgas with embedded test functionality does not end with verification of the chip's design. "This is merely the beginning of the useful life of that instrument," Woppman commented. "Its benefits ripple throughout chip development, including IC test and characterisation. Then, as chips are rolled onto pcbs and into systems, additional benefits - stemming from the ability of embedded instruments to measure and monitor performance characteristics – are achieved throughout the product life cycle of the system."

The trend towards embedded processors in fpgas adds another level of complexity to debug requiring not only fpga style debug, but also software debug for the code implemented on the processor, in the fpga. The ability to determine failure modes and even predict them is gaining momentum in system management support. The ability to read back time stamped system parameters about board operation is invaluable to failure analysis.

Lockhart concluded: "By analysing how a particular parameter varies over the life of the board, it's possible to predict a failure before it occurs, thereby increasing system uptime. Using an industrial motor control example, a customer might measure the current to the windings as well as motor vibration to determine when to bring the equipment down in a planned fashion. In industrial applications, a planned shutdown is dramatically less expensive than an unplanned one due to the cost to fix the problem as well as the possibility of lost profit from equipment shutdown. Fusion architecture enables you to send in the repairman before the board fails!" ■