

AN-6859A

Design and Application Guide for SG6859A

Abstract

The present application note describes a detailed design strategy for a high-efficiency compact flyback converter. Design considerations and mathematical equations are presented. The guidelines for printed circuit board layout are also given.

Applications

General-purpose switching mode power supplies and flyback power converters, such as:

- Battery chargers for cellular phones, cordless phones, PDAs, digital cameras, and power tools
- Power adapters for ink jet printers, video game consoles, and portable audio players
- Open-frame SMPS for TV/DVD standby and other auxiliary supplies, home appliances, and consumer electronics
- Replacements for linear transformers and RCC SMPS
- PC 5V standby power

Pin Configuration

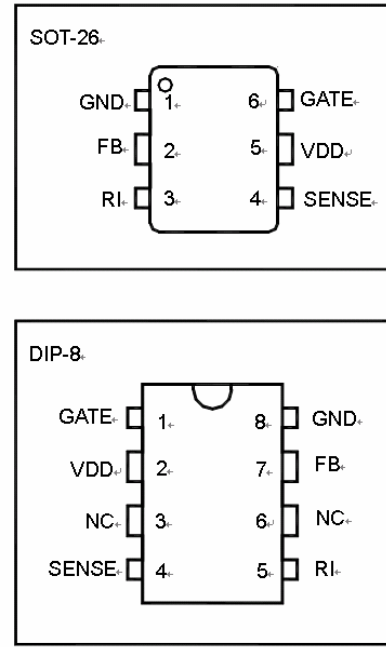


Figure 1. Pin Configuration

Typical Application

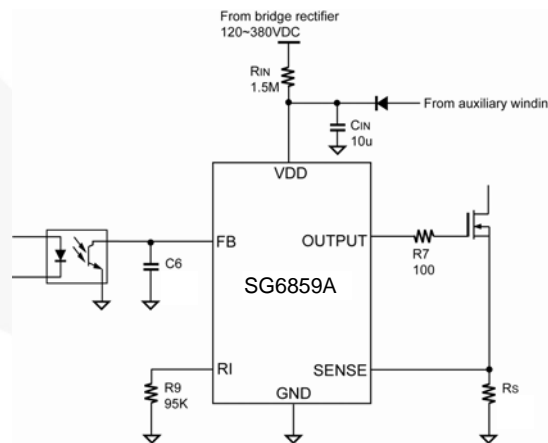


Figure 2. Application Circuit

Description

This highly integrated PWM controller provides several special enhancements designed to meet the low standby-power needs of low-power SMPS. To minimize standby power consumption, the proprietary green-mode function provides off-time modulation to linearly decrease the switching frequency under light-load conditions. This green-mode function enables the power supply to easily meet even the strictest power conservation requirements.

To protect the external power MOSFET from being damaged by excessive supply voltage, the output driver is clamped at 17V. SG6859A controllers can improve the performance and reduce the production cost of power supplies and provide a choice for replacing linear and RCC-mode power adapters. SG6859A is available in 8-pin DIP and 6-pin SOT-26 packages.

Start-up Circuitry

When the power is turned on, the input rectified voltage, V_{DC} , charges the hold-up capacitor C1 via a start-up resistor R_{IN} . As the voltage of VDD pin reaches the start threshold voltage V_{DD-ON} , SG6859 activates the entire power supply.

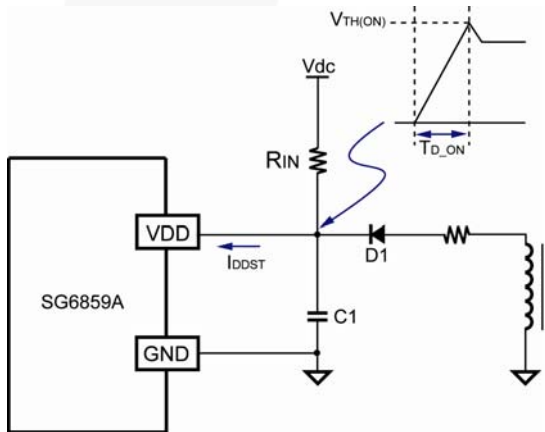


Figure 3. Circuit Providing Power to SG6859A

The maximum power-on delay time is determined as:

$$V_{DD-ON} = (V_{dc} - I_{DD-ST} \cdot R_{IN}) \left[1 - e^{-\frac{T_{D-ON}}{R_{IN} \cdot C1}} \right] \quad (1)$$

where:

I_{DD-ST} is the start-up current of SG6859A, and

T_{D-ON} is the power-on delay time of the power supply.

Due to the low start-up current, a large R_{IN} such as 1.5M Ω can be used. With a hold-up capacitor of 10 μ F/50V, the power-on delay T_{D-ON} is less than 2.8s for 90V_{AC} input.

The FB input

This pin is designed for feedback control and to activate the green-mode function. Figure 4 is a typical feedback circuit consisting mainly of a shunt regulator and an photo-coupler. R1 and R2 form a voltage divider for the output voltage regulation. R3 and C1 are adjusted for control-loop compensation. A small-value RC filter (e.g. $R_{FB}=47\Omega$, $C_{FB}=1nF$) placed from the FB pin to GND can increase stability. The maximum source current on the FB pin is 1.5mA. The phototransistor must be capable of sinking this current to pull the FB level down at no load. The value of the biasing resistor R_b is determined as follows.

$$\frac{V_o - V_D - V_Z}{R_b} \cdot K \geq 1.5mA \quad (2)$$

where:

V_D is the drop voltage of a photodiode, about 1.2V;

V_Z is the minimum operating voltage of the shunt regulator (typical: 2.5V);

K is the current transfer rate (CTR) of the photo-coupler.

For an output voltage $V_o=5V$, with CTR=100%, the maximum value of R_b is 860 Ω .

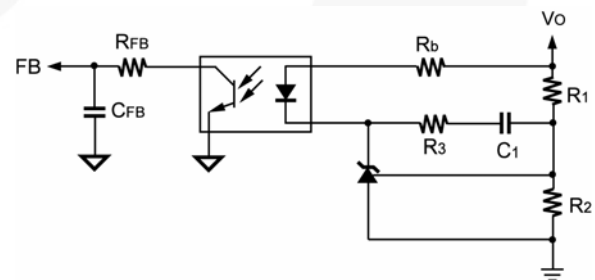


Figure 4. Feedback Circuit

Recommended R_{FB} is from 10 to 100 Ω .

C_{FB} is from 1 to 10nF.

Oscillator & Green Mode Operation

One external resistor, R_1 , connected between RI and GND pins is used to program the PWM frequency of the SG6859A. The approximated formula is:

$$f_{osc} \text{ (KHz)} = \frac{6650}{R_1 \text{ (K}\Omega)} \quad (3)$$

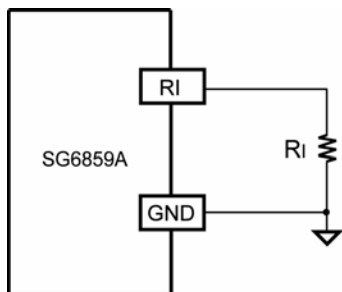


Figure 5. Setting PWM Frequency

The recommended f_{osc} is from 50 to 80KHz.

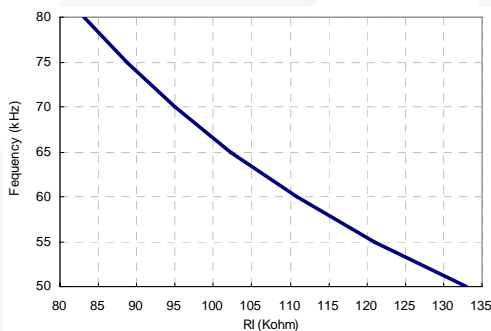


Figure 6. R_1 vs. Frequency

The proprietary green-mode function provides off-time modulation to reduce the PWM frequency at light-load and no-load conditions. The feedback voltage of the FB pin is taken as a reference. When the feedback voltage is lower than about 2.85V, the PWM frequency decreases. Because most losses in a switching-mode power supply are proportional to the PWM frequency, the off-time modulation reduces the power consumption of the power supply at light-load and no-load conditions. For a typical case of $R_1 = 95\text{K}\Omega$, the PWM frequency is 70KHz at nominal load, and decreases to 20KHz at light load, about 2/7 of the nominal PWM frequency. The power supply enters “Adaptive off-time modulation” in zero-load conditions.

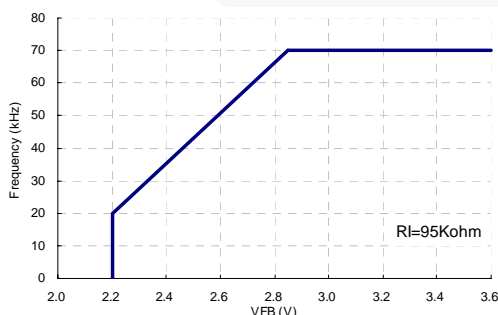


Figure 7. PWM Frequency vs. FB Voltage

A frequency hopping function improves the system EMI performance. The PWM switching frequency hops between 70KHz \pm 4.9KHz (Hopping Range). The hopping period (t_{HOP}) is around 3.7ms ($R_1=95\text{K}\Omega$).

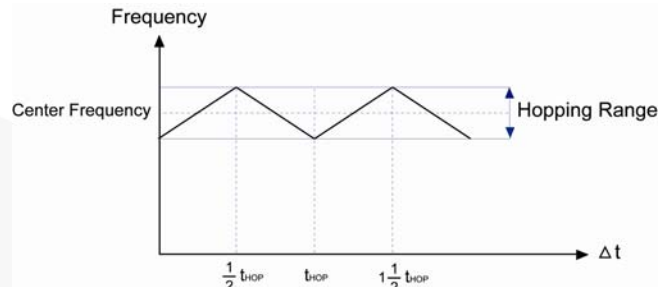


Figure 8. Frequency Hopping

Built-in Slope Compensation

A flyback converter can be operated in discontinuous current mode (DCM) or continuous current mode (CCM). There are many advantages to operating in CCM. With the same output power, a converter in CCM exhibits smaller peak inductor currents than in DCM; therefore, a small-sized transformer and a low-rated MOSFET can be applied. On the secondary side of the transformer, the rms output current of DCM can be up to twice that of CCM. Larger wire gauge and output capacitors with larger ripple current ratings are required. DCM operation also results in higher output voltage spikes. A large LC filter must be added; therefore, a flyback converter in CCM achieves better performance with lower component cost.

Despite the above advantages of operating in CCM, there is one concern – stability. Operating in CCM, the output power is proportional to the average inductor current, while the peak current is controlled. This causes a well-known sub-harmonic oscillation when the PWM duty cycle exceeds 50%. Adding slope compensation (reducing the current-loop gain) is an effective way to prevent this oscillation. The SG6859A introduces a synchronized positive-going ramp (V_{SLOPE}) in every switching cycle to stabilize the current loop. The sensed voltage, together with this slope compensation signal (V_{SLOPE}), is fed into the non-inverting input of the PWM comparator. The resulting voltage is compared with the FB signal to adjust the PWM duty cycle, such that the output voltage is regulated. The SG6859A aids design of cost-effective, highly efficient, and compact-sized flyback power supplies operating in CCM without adding any external components.

The positive ramp added is:

$$V_{SLOPE} = V_{SL} \cdot D \quad (4)$$

where

$$V_{SL} = 0.33\text{V};$$

D = Duty cycle

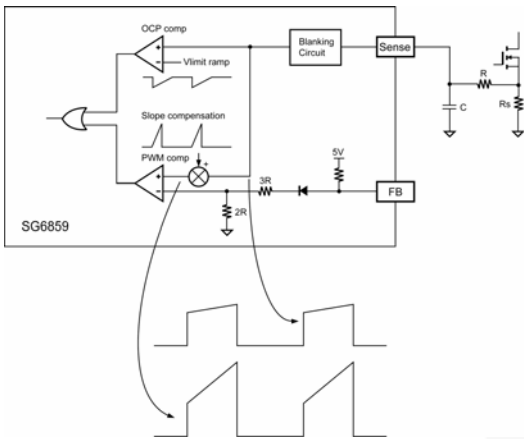


Figure 9. Synchronized Slope Compensation

Constant Output Power Limit

The maximum output power of a flyback converter can generally be determined from the current-sense resistor R_S . When the load increases, the peak inductor current increases accordingly. Once the output current arrives at the protection value, the OCP comparator dominates the current control loop. OCP occurs when the current-sense voltage reaches the threshold value. The output GATE driver is turned off after a small propagation delay, t_{PD} . The delay time results in unequal power-limit level under universal input. In the SG6859A, a saw-tooth power-limiter (saw limiter) is designed to solve the unequal power-limit problem. As shown in Figure 10, the saw limiter is designed as a positive ramp ($V_{limit\ ramp}$) signal and is fed to the inverting input of the OCP comparator. This results in a lower current limit at high-line inputs than at low-line inputs. With fixed propagation delay, t_{PD} , the peak primary current would be the same for various line input voltages; therefore, the maximum output power can practically be limited to a constant value within a wide input voltage range without adding any external circuitry.

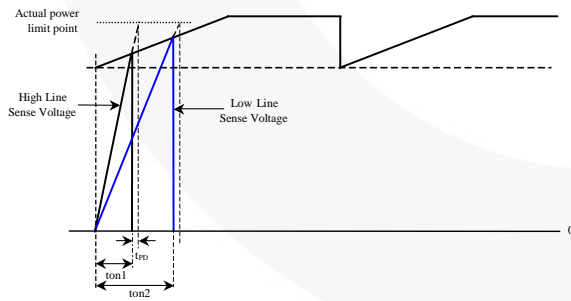


Figure 10. Constant Power Limit Compensation

V_{DD} Over-voltage Protection (OVP)

V_{DD} over-voltage protection prevents damage due to over-voltage conditions. When the voltage V_{DD} exceeds the internal threshold due to abnormal conditions, PWM output is turned off until the V_{DD} voltage drops below the UVLO, then starts up again. Over-voltage conditions are usually caused by open feedback loops.

Short-Circuit Protection

When the output of a flyback power supply is shorted, the primary V_{DD} decreases due to the coupling polarity between the auxiliary winding and the secondary winding of a transformer. When V_{DD} drops below UVLO level, the power supply enters hiccup operation mode and limits the output power. However, it is possible that the V_{DD} voltage remains higher than the UVLO level even if the output is shorted. This occurs when the coupling between the auxiliary and the primary winding is too good; therefore, the construction of the transformer becomes a dominant factor. The recommended construction layout is to increase the insulation thickness for the auxiliary winding and place the primary auxiliary winding in one side of the bobbin. For low-output voltage applications, using a low dropout voltage diode and a larger secondary winding can also help.

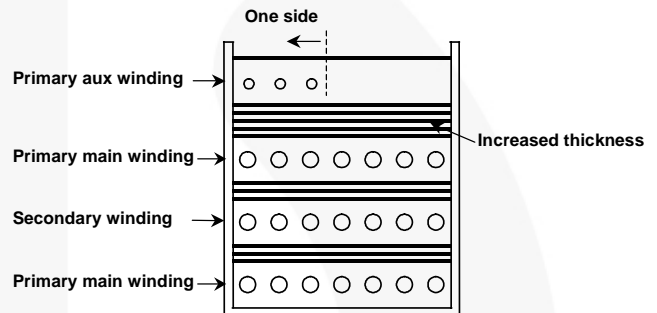


Figure 11. Transformer Construction

Leading-Edge Blanking (LEB)

A voltage signal proportional to the MOSFET current develops on the current-sensing resistor, R_S . Each time the MOSFET is turned on, a spike induced by the diode reverse recovery and by the output capacitances of the MOSFET and diode, appears on the sensed signal. Inside the SG6859A, a leading-edge blanking time of about 320ns is introduced to avoid premature termination of the MOSFET by the spike. Therefore, only a small-value RC filter (e.g. 100Ω+ 470pF) is required between the SENSE pin and R_S . Still, a non-inductive resistor for the R_S is recommended.

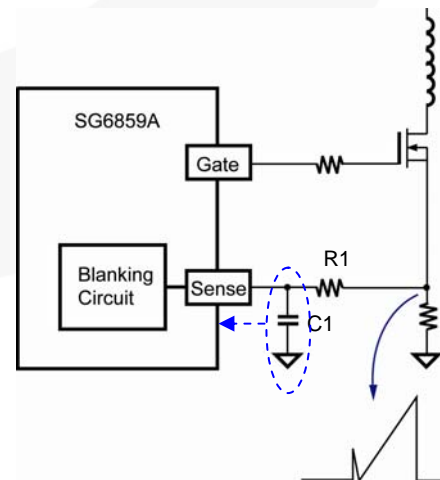


Figure 12. Turn-on Spike

The recommended R1 is from 100 to 200Ω.

C1 is from 100 to 470pF.

C1 capacitor needs to be close to the SENSE pin and GND pin of SG6859A.

Open-Loop Protection

When an open-loop failure happens, the voltage on the FB pin rises rapidly owing to the internal pull-high circuitry. Once the FB voltage level goes beyond 4.6V (V_{FB-OL}) for about 56ms (t_{D-OLP}), the SG6859A stops PWM output pulses. As the PWM output is turned off, V_{DD} begin decreasing. After V_{DD} goes below the turn-off threshold, the SG6859A is totally shut down and FB voltage drops to zero. Then V_{DD} is charged up to the start-up threshold voltage of 16.5V through the start-up resistor until PWM output is restarted. This hiccup mode protection happens repeatedly as long as the open-circuit failure persists.

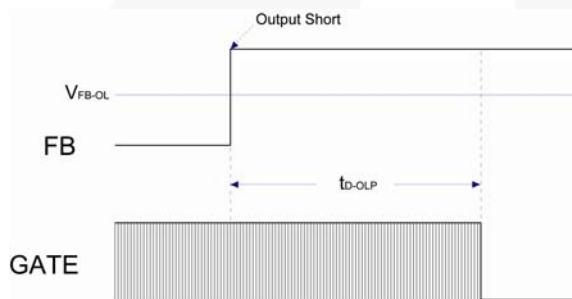


Figure 13. FB Open-loop Protection

GATE Drive

The output stage is a fast totem-pole driver that can drive a MOSFET gate directly. It is also equipped with a voltage clamping Zener diode to protect the MOSFET from damage caused by undesirable over-drive voltage. The output voltage is clamped at 17V. An internal pull-down resistor is used to avoid a floating state of the gate before startup. A gate drive resistor in the range of 47 to 100Ω is recommended. This resistor limits the peak gate drive current and provides damping to prevent oscillations at the MOSFET gate terminal.

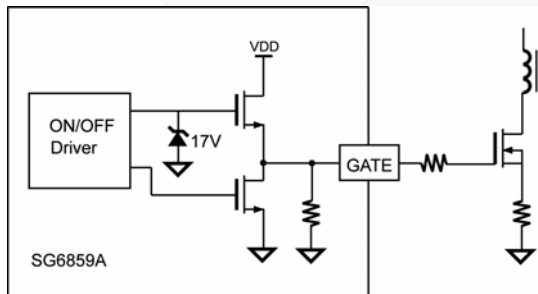


Figure 14. GATE Drive

Lab Note

Before reworking or soldering/de-soldering on the power supply, it is suggested to discharge the primary capacitors by an external bleeding resistor. Otherwise, the PWM IC may be destroyed by external high-voltage during soldering or de-soldering.

This device is sensitive to ESD discharge. To improve the production yield, the production line should be ESD protected in accordance to ANSI ESD S1.1, ESD S1.4, ESD S7.1, ESD STM 12.1, and EOS/ESD S6.1.

Printed Circuit Board (PCB) Layout

High-frequency switching current/voltage make PCB layout a very important design issue. Good PCB layout minimizes excessive EMI and helps the power supply survive during surge/ESD tests.

General Guidelines

- To get better EMI performance and reduce line frequency ripples, the output of the bridge rectifier should be connected to capacitor C1 first, then to the switching circuits.
- The high-frequency current loop is in C1 – Transformer – MOSFET – RS – C1. The area enclosed by this current loop should be as small as possible. Keep the traces (especially 4→1) short, direct, and wide. High-voltage traces related to the drain of the MOSFET and the RCD snubber should be kept far away from control circuits to prevent unnecessary interference. If a heat sink is used for the MOSFET, connect this heat sink to ground.
- As indicated by 3, the ground of control circuits should be connected first before any other circuitry.
- As indicated by 2, the area enclosed by the transformer auxiliary winding, D1, and C2 should also be kept small. Place C2 close to the SG6859A for good decoupling.

Two suggestions for ground connections, with different pros and cons, are offered.

- GND3→2→4→1: This should avoid common impedance interference for the sense signal.
- GND3→2→1→4: This should be better for ESD tests, where the earth ground is not available on the power supply. Regarding the ESD discharge path, the charges go from secondary through the transformer's stray capacitance to GND2 first. Then the charges go from GND2 to GND1 and back to the mains. It should be noted that control circuits should not be placed in the discharge path. Point discharges for common choke can decrease the high-frequency impedance and help increase ESD immunity.
- Should a Y-cap between primary and secondary be required, it is suggested to connect this Y-cap to the positive terminal of C1 (V_{DC}). If this Y-cap is connected to primary GND, it should be connected to the negative terminal of C1 (GND1) directly. The point discharge of this Y-cap also helps with ESD; however, the distance between these two points should be at least 5mm according to safety requirements.

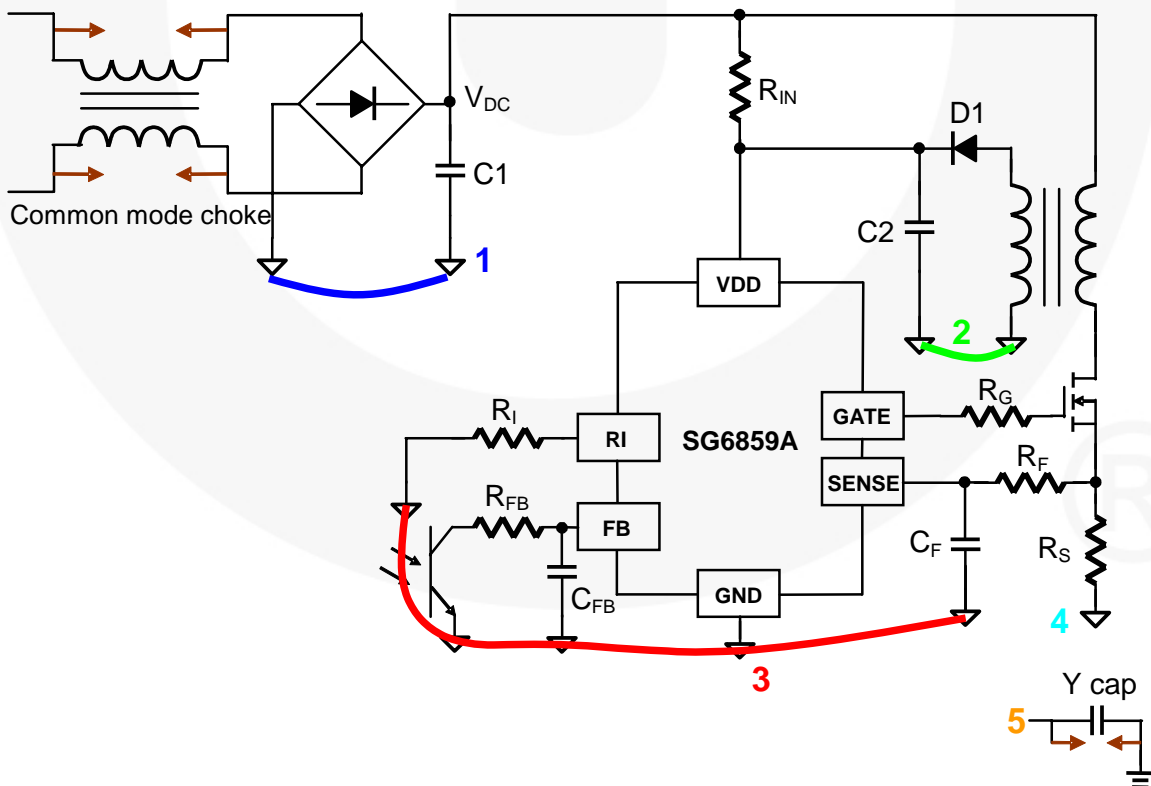


Figure 15. Layout Considerations



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