



## PFC Inductor

The switching frequency  $f_{SW}$ , the output power  $P_{OUT}$ , the efficiency  $\eta$ , maximum ripple current  $\Delta I$ , and the minimum input voltage  $V_{IN.min}$  should be defined before determining the inductance of the PFC inductor. The following equations are utilized to determine the inductance of the PFC inductor. Normally, the maximum ripple current is set at 20~30% of maximum input current.

$$\Delta I = \frac{\sqrt{2} \times P_{OUT} \times 0.3}{V_{IN.min} \times \eta} \quad (1)$$

$$D = 1 - \frac{V_{IN.min} \times \sqrt{2}}{V_{OUT}} \quad (2)$$

$$V = L \frac{di}{dt} \quad (3)$$

$$L = \frac{V_{IN.min} \times \sqrt{2} \times D_{max}}{\Delta I \times f_{SW}} \quad (4)$$

For a 300W power-factor-correction circuit,  $\eta=0.75$ ,  $V_{IN.min}=90V_{AC}$ ,  $f_{SW}=65KHz$ ,  $V_{OUT}=390V$ ,  $\Delta I=1.89A$ ,  $D=0.674$ , and  $L=700\mu H$ .

## PFC Capacitor

One advantage of using interleaving switching in the PFC and PWM stages is that it reduces the switching noise. The ESR requirement for boost capacitor is also reduced.

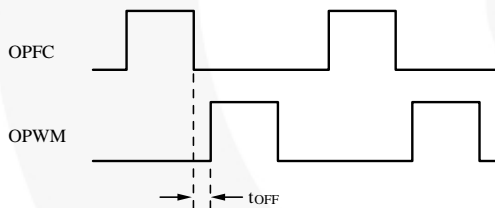


Figure 2. Interleaving Switching

The boost capacitor value is chosen to remain at the hold-up time of output voltage in the event that the line voltage is removed.

$$C_{OUT} > \frac{2 \times P_{OUT} \times t_{hold-up}}{(V_{OUT(normal)} - V_{ripple})^2 - V_{OUT.min}^2} \times \frac{1}{\eta_{PWM}} \quad (5)$$

$V_{OUT.min}$  represents the minimum output voltage in accordance with the requirement of the specification.

For a 300W power supply, the capacitor is determined as follows

$$C_{OUT} > \frac{2 \times 300W \times 28ms}{(390 - 20)^2 - 90^2} \times \frac{1}{0.85} = 153\mu F \quad (6)$$

Because the capacitor includes a  $\pm 20\%$  variation, the 180 $\mu F$  capacitor has been chosen.

## Boost Rectifier and Switch

A fast reverse-recovery time of the boost diode is required to reduce power losses and EMI. In addition, a 500V

voltage rating has been chosen in order to withstand 390V boosts potential. The average current and peak current flow through the boost diode and switch, respectively, are determined by:

$$I_{avg} = \frac{2 \times \sqrt{2} \times P_{OUT}}{\pi \times V_{RMS(Brownout)} \times \eta} \quad (7)$$

$$I_{avg} = \frac{2 \times \sqrt{2} \times 300}{\pi \times 75 \times 0.7} = 5.15A$$

$$I_{PEAK} = \sqrt{2} \times \frac{P_{OUT}}{V_{RMS(Brownout)} \times \eta} \quad (8)$$

$$I_{PEAK} = \sqrt{2} \times \frac{300}{75 \times 0.7} = 8.08A$$

## Oscillator and Green-Mode Operation

The resistor  $R_I$  connected from the RI pin to GND programs the switching frequency of SG6905.

$$f_{SW} = \frac{1560}{R_I(k\Omega)} (KHz) \quad (9)$$

For example, a 24k $\Omega$  resistor  $R_I$  results in a 65KHz switching frequency. The recommended range for the switching frequency of SG6905 is 33~100KHz.

SG6905 provides an off-time modulation to reduce the switching frequency in light-load and no-load conditions. The feedback voltage of the FBPWM pin can be used as a reference. When the feedback voltage falls below approximately 2.0V, the switching frequency decreases accordingly. Most of the losses in the switching-mode power supply are proportional to the switching frequency. Therefore, the off-time modulation of SG6905 reduces the power consumption of the power supply in light-load and no-load conditions. For a typical case in which  $R_I = 24k\Omega$ , the switching frequency is 65kHz at the nominal load, which decreases to 21KHz at the light load. The switching signal is disabled if the switching frequency falls below 21KHz, thereby avoiding acoustic noises. The function to reduce the PWM stage-switching frequency is enabled when the PFC stage does not work. After the PFC stage resumes working, the function to reduce the PWM stage-switching frequency is disabled.

Due to stability issues, a capacitor connecting the RI pin to GND is not suggested.

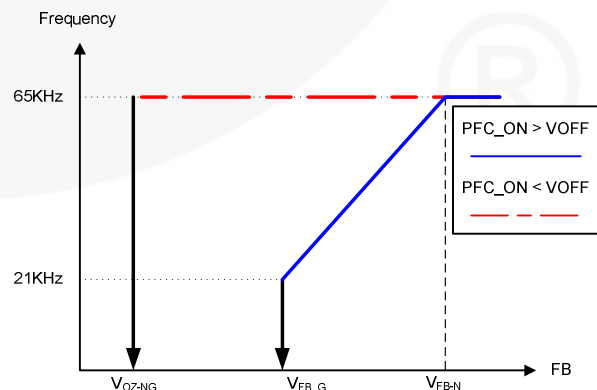


Figure 3. Switch Frequency vs. FB Voltage

## I<sub>AC</sub> Signal

Figure 4 shows that the I<sub>AC</sub> pin is connected to the input voltage via a resistor. A current I<sub>AC</sub> is used for the PFC multiplier.

$$I_{AC(PEAK)} \approx \frac{V_{IN(PEAK)}}{R_{AC}} \quad (10)$$

For wide-range input,

$$V_{IN(PEAK)} = 264V \times \sqrt{2} = 374V \quad (11)$$

The linear range of I<sub>AC</sub> is 0~360μA. A 1.2MΩ resistor is suggested for a wide input range (90~264V<sub>AC</sub>).

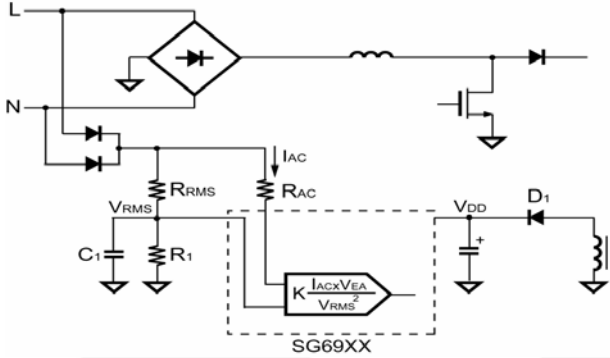


Figure 4. The I<sub>ac</sub> Signal

## Line-Voltage Detection (V<sub>RMS</sub>)

Figure 4 also indicates the resistive divider from a low-pass filter connected to the V<sub>RMS</sub> pin for line-voltage detection. The V<sub>RMS</sub> input is used for the PFC multiplier and brownout protection.

For a sine wave input voltage, the voltage on the V<sub>RMS</sub> pin is directly proportional to the input voltage. In order to achieve brownout protection, SG6905's PFC stage is disabled after a 195ms time delay once the V<sub>RMS</sub> voltage drops below 0.8V. The PWM stage is protected through the open loop detection on the FBPWM pin when the PFC stage's output voltage is too low. After that, SG6905 turns off. When the V<sub>RMS</sub> voltage increases above 0.99V, SG6905 restarts in accordance with the power-on sequence of the PFC and PWM stages.

For example, brownout protection is set at 75V<sub>AC</sub>. The R<sub>RMS</sub> and R<sub>1</sub> can be determined as follows:

$$V_{IN(Mean)} = V_{IN} \times \sqrt{2} \times \frac{2}{\pi} \quad (12)$$

$$V_{RMS} = \frac{R_1}{R_1 + R_{RMS}} \times V_{IN} \times \sqrt{2} \times \frac{2}{\pi} \quad (13)$$

The threshold of V<sub>RMS</sub>=0.8V; assuming that R<sub>RMS</sub>=4.8MΩ and V<sub>IN</sub>=75V<sub>AC</sub>, the value of R<sub>1</sub> is 56.8kΩ

## PFC Operation

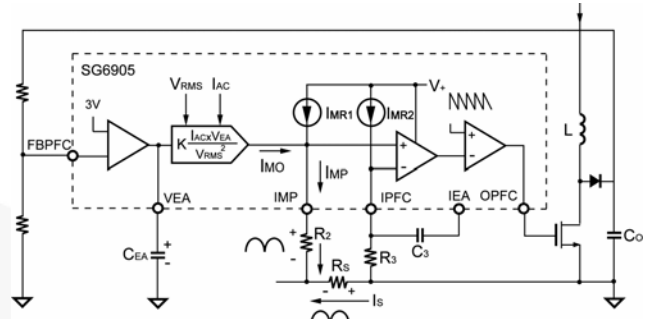


Figure 5. Current-Feedback Circuit

The current output from the switching-charge multiplier/divider can be expressed as:

$$I_{MO} = K \times \frac{I_{AC} \times V_{EA}}{V_{RMS}^2} (\mu A) \quad (14)$$

Referring to Figure 5, the current output from the IMP pin, I<sub>MP</sub>, is the summation of I<sub>MO</sub> and I<sub>MR1</sub>. The resistor R<sub>2</sub> is equipped similarly as R<sub>3</sub>. The constant-current source I<sub>MR1</sub> is identical to I<sub>MR2</sub>. Both are used to bias (pull up) the operating point of the I<sub>MP</sub> and IPFC pins since the voltage across R<sub>S</sub> goes negative with respect to the ground.

Through the differential amplification of the signal across R<sub>S</sub>, a better noise immunity is achieved. The output of IEA compared with an internal sawtooth generates a switching signal for PFC. Through the feedback loop of the average-current-mode control, the input current I<sub>S</sub> is proportional to I<sub>MO</sub>.

K is the current transfer rate (CTR) of the photo-coupler.

For an output voltage V<sub>OUT</sub>=5V, with CTR=100%, the maximum value of R<sub>b</sub> is 860Ω.

$$I_{MO} \times R_2 = I_S \times R_S \quad (15)$$

According to equation 15, the minimum value of R<sub>2</sub> and maximum value of R<sub>S</sub> can be determined. The I<sub>MO</sub> should be estimated under its specified maximum value.

Other concerns in determining the value of the sense resistor R<sub>S</sub> are lower resistance, R<sub>S</sub> causes a lower power consumption for higher resistance, and R<sub>S</sub> has a higher resolution for achieving a lower total harmonic distortion (THD) of the input current. Using a current transformer (CT) is recommended instead of R<sub>S</sub> to improve the efficiency of high-power converters.

For a 300W power supply, the power consumption of  $R_S=0.1\Omega$  is:

$$P_{RS} = \left(\frac{300W / 0.75}{90}\right)^2 \times 0.1 = 1.98W \quad (16)$$

$R_2$  and  $R_3$  can be determined as follows: (The brownout protection threshold is 75V.)

$$I_{MAX} = \frac{300W / 0.7}{75V} * \sqrt{2} = 8.08A \quad (17)$$

$$V_{IPFC} = 50\mu A * 3.9k\Omega = 0.195V \quad (18)$$

$$I_{MO} + I_{MR1} = \frac{0.195 - (-8.08A * 0.1\Omega)}{3.9k\Omega} = 257\mu A \quad (19)$$

$$I_{MO} = 257 - 50 = 207\mu A$$

The results indicate that the  $R_S$ ,  $R_2$ , and  $R_3$  values fit when providing 300W output.

### Cycle-By-Cycle Current Limiting

SG6905 provides cycle-by-cycle current limiting for both PFC and PWM stages. Figure 6 shows the peak current limit for the PFC stage. The switching signal of the PFC stage is turned off immediately once the voltage on the ISENSE pin goes below the threshold voltage  $V_+$ .

The voltage of  $V_{RMS}$  determines the threshold voltage  $V_+$ . The correlation of the threshold voltage  $V_+$  and  $V_{RMS}$  is shown in Figure 6. The amplitude of the constant current  $I_P$  shown in Figure 6 is determined by a reference current  $I_T$ , in accordance with the following equation:

$$I_P = 2 \times I_T = 2 \times \frac{1.2V}{R_I} \quad (20)$$

Therefore the peak current of  $I_S$  can be expressed as:

$$I_{S\_PEAK} = \frac{(I_P \times R_P) - 0.2V}{R_S} \quad (21)$$

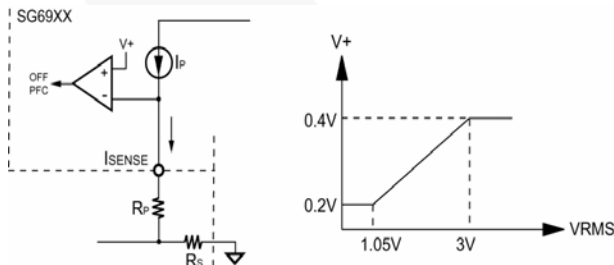


Figure 6. Current Limit

### PFC Voltage Loop

There are two major concerns when compensating the voltage-loop error amplifier ( $V_{EAO}$ ): stability and transient response. Optimizing interaction between stability and transient response requires that the error amplifier's open-loop crossover frequency be half that of the line frequency, or 23Hz for a 47Hz line (lowest anticipated international power frequency). The gain vs. input voltage of the SG6905's voltage-error amplifier ( $V_{EAO}$ ) has a specially shaped non-linearity, so that under steady-state operating conditions the transconductance of the error amplifier is at a local minimum. Rapid perturbation in line or load conditions causes the input to the voltage error amplifier ( $V_{FB}$ ) to deviate from its 3V (nominal) value. If this happens, the transconductance of the voltage error amplifier increases significantly. This raises the gain-bandwidth product of the voltage loop, resulting in a much more rapid voltage-loop response to such perturbations than would occur with conventional linear characteristics.

The voltage-loop gain(s) is given by:

$$\begin{aligned} &= \frac{\Delta V_{OUT}}{\Delta V_{EAO}} \times \frac{\Delta V_{FB}}{\Delta V_{OUT}} \times \frac{\Delta V_{EAO}}{\Delta V_{FB}} \\ &\approx \frac{P_{IN} \times 3}{V_{OUTDC}^2 \times \Delta V_{EAO} \times S \times C_{DC}} \times GM_V \times Z_C \end{aligned} \quad (22)$$

where:

$Z_C$ : Compensation network for the voltage loop.

$GM_V$ : Transconductance of  $V_{EAO}$ .

$P_{IN}$ : Average PFC input power.

$V_{2OUTDC}$ : PFC boost output voltage (typical designed value is 380V).

$C_{DC}$ : PFC boost output capacitor.

The average total input power can be expressed as:

$$\begin{aligned} P_{IN} &= V_{IN}(rms) \times I_{IN}(rms) \\ &\propto V_{RMS} \times I_{MO} \propto V_{RMS} \times \frac{I_{AC} \times V_{EA}}{V_{RMS}} \\ &\propto V_{RMS} \times \frac{V_{IN} \times V_{EA}}{R_{AC}^2} = \sqrt{2} \times \frac{V_{EA}}{R_{AC}} \end{aligned} \quad (23)$$

From equation (23),  $V_{EA}$ , the output of the voltage-error amplifier, actually controls the total input power and hence the power delivered to the load.

### PFC On/Off

PFC\_ON controls the PFC stage whether it works normally or not. The PFC stage is disabled when the voltage of PFC\_ON surpasses 2.45V. The PFC stage remains active while the voltage of PFC\_ON is low. At this point, OPFC can work normally, and the RDY pin pulls high.

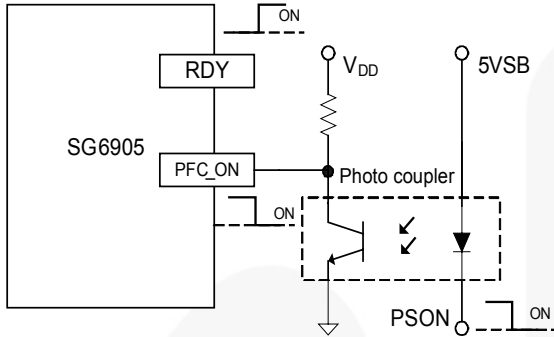


Figure 7. PFC\_ON Pin

### RDY-Pin Application

The state of RDY is determined by the PFC\_ON and FBPFC pins. The RDY pin rises to high when PFC\_ON pulls low and the voltage of the FBPFC pin is higher than 2.7V. SG6905 can enable other PWM IC to work or not according to the RDY signal.

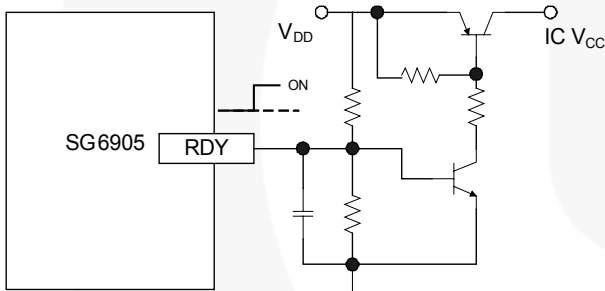


Figure 8. RDY-Pin Application

### PWM Section

#### Soft Start of the PWM Stage

The soft-start pin has been developed to control the rising time of the output voltage and to prevent overshoot during power on. The soft-start capacitor value for the soft-start period  $t_{SS}$  is given by:

$$C_{SS} = t_{SS} \times \frac{I_{SS}}{V_{OZ}} \tag{24}$$

Where  $V_{OZ}$  represents the zero-duty threshold of FBPWM voltage.

### Leading-Edge Blanking

A voltage signal develops on the current-sense resistor  $R_S$  to represent the switching current of the MOSFET. Each time the MOSFET is turned on, a spike is produced, caused by the diode-reverse-recovery time and the parasitic capacitances of the MOSFET, and inevitably appears on the sensed signal. SG6905 has a built-in leading-edge blanking

time of about 120ns to avoid premature termination of the MOSFET by the spike. Therefore, only a small-value RC filter (e.g., 100Ω + 47pF) is required between the IPWM pin and  $R_S$  to prevent negative spike into the IPWM pin. A non-inductive resistor for  $R_S$  is recommended.

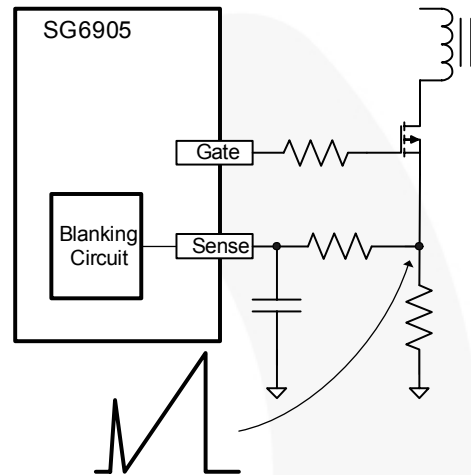


Figure 9. C<sub>s</sub> Turn On

### Flyback PWM and Slope Compensation

As shown in Figure 10, peak-current-mode control is utilized for Flyback PWM. SG6905 inserts a synchronized ramp at the beginning of each switching cycle. This built-in slope compensation ensures stable operation for continuous-current-mode operation.

When the IPWM voltage across the sense resistor reaches the threshold voltage (0.9V), the OPWM is turned off after a small propagation delay,  $t_{PD-PWM}$ .

To improve stability or prevent sub-harmonic oscillation, a synchronized positive-going ramp is inserted at every switching cycle.

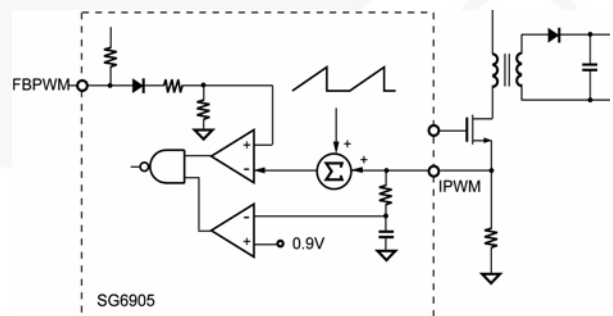


Figure 10. Peak-Current-Control Loop

## Output Driver of OPFC & OPWM

SG6905's OPFC and OPWM create a fast totem-pole gate driver able to directly drive an external MOSFET. An internal zener diode clamps the driver voltage under 18V to protect the MOSFET from over-voltage.

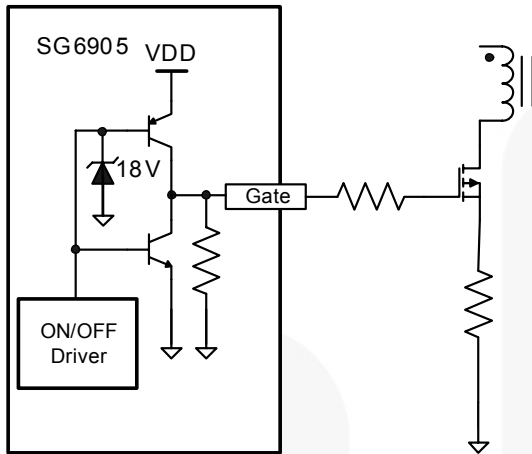


Figure 11. Gate-Driver Circuit

## OCP & SCP

SG6905's OCP and SCP have been developed based on the detection of the feedback signal on the FBPWM pin. As shown in Figure 12, when over current or short circuit occurs, FBPWM is pulled high through the feedback loop. If the FB voltage surpasses the 4.5V threshold for longer than the 56ms debounce time, SG6905 is turned off. Once the V<sub>DD</sub> falls below the turn-off threshold voltage, such as 10V, SG6905 is under-voltage-lockout (UVLO) shut down. Using the start-up resistor, V<sub>DD</sub> is charged (up to the turn-on threshold voltage of 16V) until SG6905 is enabled again. If the over-loading condition still exists, the protection takes place repeatedly. This prevents the power supply from being overheated during over-loading conditions. The 600ms time-out signal prevents SG6905 from being latched off when the input voltage is fast on/off.

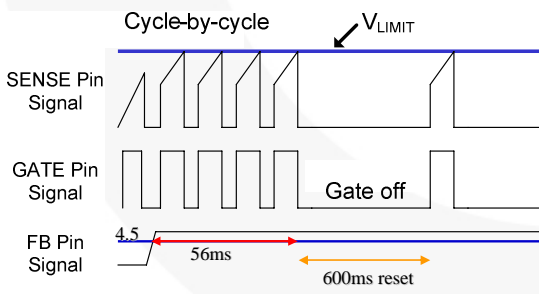


Figure 12. OCP-Detection Waveform

## OTP

SG6905 provides an OTP pin for over-temperature protection. A constant current is outputted from this pin. When R<sub>i</sub> equals 24kΩ, the magnitude of the constant current is 100μA. An external NTC thermistor must be connected from this pin to the ground, as shown in Figure 13. When the OTP voltage drops below 1.2V, SG6905 is disabled until the OTP voltage exceeds 1.4V. Preventing OTP error caused by noise disturbance can be addressed by adding a capacitor.

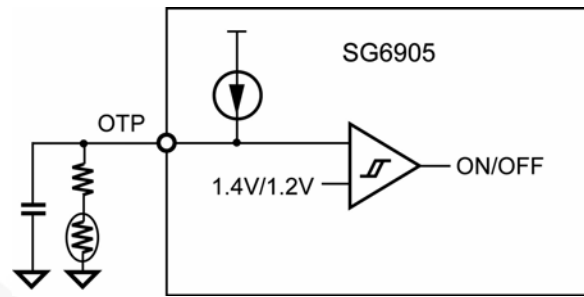


Figure 13. OTP-Application Circuit

## Flyback-Transformer Design

The turn ratio  $n = N_p/N_s$  is an important parameter for a flyback-power converter. It affects the maximum duty of the switching signal when the input voltage is at a minimum value. Moreover, it influences the voltage stresses of the MOSFET and the secondary rectifier.

In equations 25 and 26, if  $n$  increases, the voltage stress of the MOSFET is increased. However, the voltage stress of the secondary rectifier is decreased accordingly.

$$V_{DS,max} = V_{IN,max} + n \times (V_{OUT} + V_F) \quad (25)$$

$$V_{AK,max} = \frac{V_{IN,max}}{n} + V_{OUT} \quad (26)$$

Where  $V_F$  is the forward voltage of output diode  $V_{IN,max} = 390V$ .

In the maximum duty cycle and minimum input voltage at full load, the transformer inductance can be calculated as:

$$D_{max} = \frac{n \times (V_{OUT} + V_F)}{V_{IN,min} + n \times (V_{OUT} + V_F)} \quad (27)$$

$$L_p = \frac{\eta \times (V_{IN,min} \times D_{max})^2}{2 \times P_{OUT} \times f_s \times Br} \quad (28)$$

Where, Br is how much percentage of the output power flows into CCM in the low-line input voltage. Normally, the Br is set at 30~50% when  $V_{IN,min} = 90V$ .

Figure 14 shows the primary-current waveform. Once the inductor  $L_p$  is determined, the primary peak current  $I_{PEAK}$  and average current  $I_{av}$  at the full-load and low-line input voltage can be expressed as:

$$I_{avg} = \frac{P_{OUT}}{\eta \times V_{IN,min} \times D_{max}} \quad (29)$$

$$\Delta I_p = \frac{V_{IN,min}}{L_p} \times D_{max} \times t_s \quad (30)$$

$$I_{PEAK} = \frac{\Delta I_p}{2} + I_{avg} \quad (31)$$

$$I_{sq} = I_{PEAK} - \Delta I_p \quad (32)$$

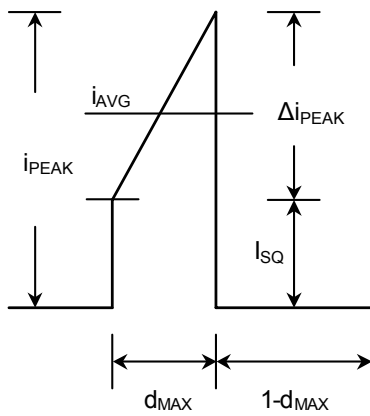


Figure 14. Primary-Current Waveform

From Faraday's law, the turns of primary side can be expressed as:

$$N_p = \frac{L_p \times I_{PEAK}}{B_{max} \times A_e} \cdot 10^8 \quad (33)$$

The turns of auxiliary winding can be expressed as:

$$N_{aux} = \frac{N_p \times (V_{DD} + V_{fa}) \times (1 - D_{max})}{V_{IN.min} \times D_{max}} \quad (34)$$

where  $V_{DD}$  is set to around 12V and  $V_{fa}$  is the forward voltage of the  $V_{DD}$  rectifier diode.

### Transformer Winding Structure

The auxiliary winding of the transformer has been developed to provide a power source ( $V_{DD}$  voltage) to the control circuit. In order to produce a regulated  $V_{DD}$  voltage, the reflected voltage of the auxiliary winding is designed to correlate to the output voltage of the secondary winding. However, a switching voltage spike caused by the leakage inductance of the primary winding can be coupled to the auxiliary winding to increase the  $V_{DD}$  voltage in response to the increase of the load.

When the  $V_{DD}$  voltage increases beyond the voltage of the over-voltage protection 24.5V, the control circuit turns off the PWM and PFC stages to protect the power supply. Therefore, the transformer windings should prevent the auxiliary winding from primary winding interference.

Figure 15 shows a transformer winding structure, including the primary winding ( $N_{p1}$ ), copper layer (shield), secondary winding ( $N_s$ ), auxiliary winding (AUX), copper layer (shield), and primary winding ( $N_{p2}$ ). Because the auxiliary winding is placed between the secondary and shield windings, it can alleviate the variation of  $V_{DD}$  voltage and prevent the  $V_{DD}$  voltage from reaching the over-voltage threshold 24.5V during normal operation.

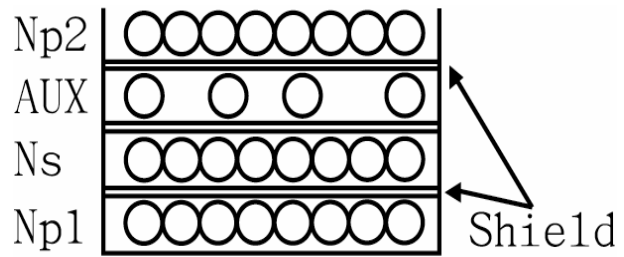


Figure 15. Winding Structure

### Lab Note

Before reworking or soldering/desoldering the power supply, discharge the primary capacitors through the external bleeding resistor. Otherwise, the PWM IC may be destroyed by external high voltage during soldering/desoldering.

This device is sensitive to ESD discharge. To improve production yield, the production line should be ESD protected according to ANSI ESD S1.1, ESD S1.4, ESD S7.1, ESD STM 12.1, and EOS/ESD S6.1.

### Printed Circuit Board (PCB) Layout

Note that SG6905 has two ground pins. Good high-frequency or RF layout practices should be followed. Avoid long PCB traces and component leads. Locate decoupling capacitors near SG6905. A resistor (5~20Ω) is recommended for connecting the series from the OPFC and OPWM to the gate of the MOSFET.

Isolating the interference between the PFC and PWM stages is also important. Figure 16 shows an example of the PCB layout. The *ground trace* connecting the AGND pin of SG6905 to the decoupling capacitor should be low impedance and as short as possible. The *ground trace 1* provides a signal ground; it should be connected directly to the decoupling capacitor  $V_{DD}$  and/or to SG6905's AGND pin. The *ground trace 2* shows that the AGND pins should connect to the PFC output capacitor  $C_o$  independently. The *ground trace 3* is independently tied from the GND to the PFC output capacitor  $C_o$ . The ground in the output capacitor  $C_{OUT}$  is the major ground reference for power switching. In order to provide a good ground reference and reduce the switching noise of both the PFC and PWM stages, the *ground traces 6 and 7* should be located near one another and be of minimal impedance.

The IPFC pin is connected directly to  $R_s$  through  $R_3$  to improve noise immunity (be aware that it may be incorrectly connected to the *ground trace 2*). The IMP and ISENSE pins should also be connected directly via the resistors  $R_2$  and  $R_p$  to another terminal of  $R_s$  since the *ground traces 4 and 5* are PFC and PWM stages. The current loop should be as short as possible.

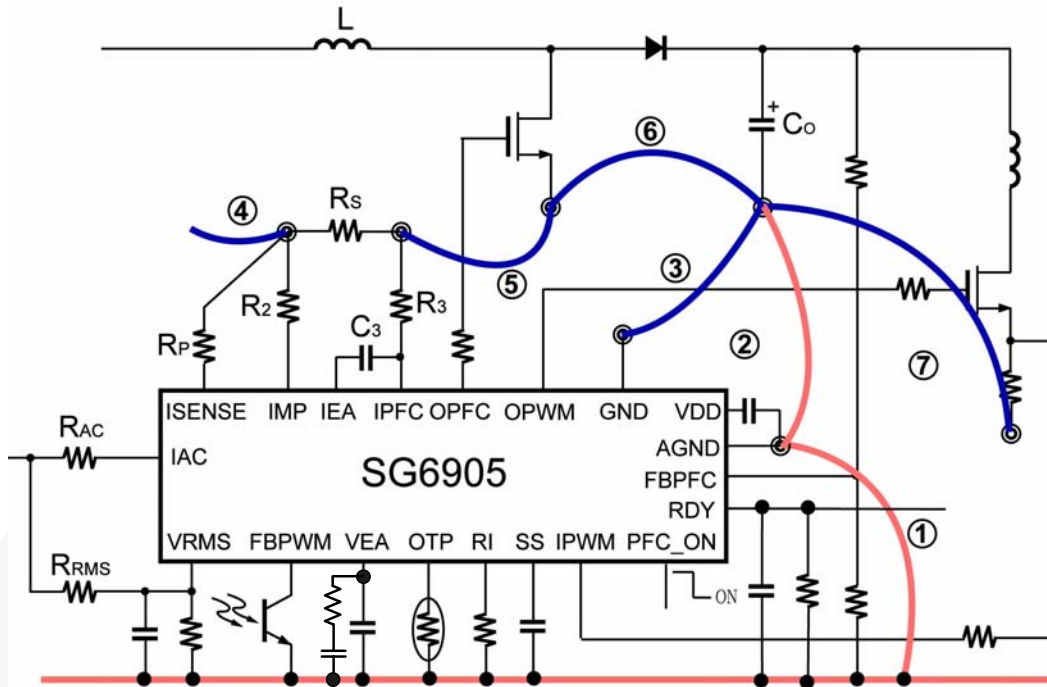


Figure 16. Layout Considerations



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