

Logging makes sense for testbench debug

The structured application of advanced logging techniques for SystemVerilog testbench debug and analysis. By Bindesh Patel and Amanda Hsiao.

SystemVerilog provides a compelling way to address the verification complexity challenge – not simply as a new language for describing complex structures, but also as a platform for driving a more efficient and realistic test of the design. It is no surprise, then, that the adoption of the language for verification purposes has been rapid. However, there is a gap when it comes to the debug and analysis of SystemVerilog testbench code. The accepted ‘dumpvars’ based techniques are not practical for the software like object oriented testbench code and their benefits in this realm are also questionable. At the end of the day, engineers do need to know what the testbench is doing at any given point in time. Thus far, engineers have been forced to revert to low level, text based message logging and subsequent manual analysis of the resulting text log files.

Structured message logging and advanced visualisation techniques

Logging – the process of recording history – has been widely used in systems and software environments and most SystemVerilog libraries in use today provide some utilities for logging information from the testbench to low-level text files that can be analysed after simulation. Engineers then correlate manually the testbench data to the design activity along the time axis. This is a painfully low-tech process with inherent disparity in the design and testbench debug flows, in which the visualisation ‘tool’ is often ‘vi’ or ‘emacs’.

However, an automated logging system level task is available that not only captures messages, but also captures severities and variable states as properties or attributes of the message. It also captures the call stack for use later in debug.

Since all data goes into the same debug database as the one used for HDL recording, the logged information can be visualised alongside other data, such as HDL value change and assertion states. Additionally, advanced visualisation techniques allow engineers to observe what is going on in the environment in standard waveforms or specialised applications such as time synchronised table (spreadsheet like) views which can be filtered, configured and so on.

Special purpose features, such as advanced filtering and highlighting, can be used to identify or colour specific messages based on some condition (or to quickly find matches based on user specified search criteria).

The automatic capture of the call stack during logging provides opportunities for further automating debug. For example, a logged message can be synchronised with the source code using drag and drop from the waveform to the source code, which could then jump to where the message originated. It can also be used to quickly set breakpoints at the right place to drive interactive simulation from the debug environment as discussed in the next section.

Logging to interactive link

While logging provides a coarse, high level view of testbench activity, interactive simulation of testbenches provides the GDB like data that is occasionally required to understand behaviour, including the values of variables at a specified point in time and detailed thread information.

By bridging the ability to log messages with an integrated design testbench debug flow, engineers can effectively use logging at the outset to determine the testbench code (location and time) that needs to be analysed in more detail. The ability to drive interactive testbench simulation from the debug environment allows for more user friendly set up, visualisation and analysis of the behaviour of the design, the testbench message logs and the testbench itself – all in the same environment. Strategies employed in the software domain can help engineers meet the challenges of testbench verification and debug. It is clear that simply extending the traditional hardware debug techniques to testbench debug is not sufficient or even feasible. Gaining insight into what is going on in the testbench during simulation requires a new approach that builds upon the logging and interactive concepts previously discussed.

The key is to make the logging process more sophisticated and automated so that most of the debug and analysis of testbench activity can be done at that level. The goal is to use an advanced logging mechanism to pinpoint the location of a problem. If the problem is identified as being on the testbench side and more details are needed, engineers would then go into a tightly integrated interactive mode.

Logging ... done properly

Logging has been widely used in systems and software. For example, operating systems log information all the time for later analysis and debug if needed. Similarly, most software systems log information. So it is no surprise that logging is a key pillar in SystemVerilog testbench debug and analysis.

Today's dominant SystemVerilog methodologies provide some basic libraries that enable users to log information from their testbench. However, the problem has been in visualising that information, whether instrumented using raw SVTB syntax, like `$display` and `printf`, or using specialised base classes. All logging done through these mechanisms typically ends up in text files.

In order to make debug of the design and testbench together a practical, efficient process, the logging mechanism must be flexible in terms of usage and the resulting output automatically captured in the same debug database as the design results (such as the *de facto* standard FSDB format). This is fundamental to enabling advanced visualisation, debug and analysis functionality. The proposed flow and usage are shown in Figure 1.

... to interactive

Interactive simulation is often the only mechanism available for delving into the details of testbench code. While logging can provide a coarse high level view of testbench activity, interactive simulation of testbenches can provide the GDB-like data that is required to understand their behaviour, such as the values of variables at a specified point in time and detailed thread information. Most simulators, when invoked in interactive mode, typically have access to all this information, albeit in a more primitive manner.

By bridging the ability to log messages with a unified design testbench debug system, engineers can effectively use logging at the outset to determine the testbench code (location and time) that needs to be analysed in more detail. With such a flow (shown in Figure 2), a logged message can be dragged and dropped into the source code view so engineers can set a breakpoint, then invoke interactive simulation in the background with the source code view of the debugger serving as the master cockpit.

In this way, engineers can drive the simulator to a specific time or breakpoint, so that values, call stacks, and thread information can be inspected (automatically or user-driven). This mode of operation is very similar to the GDB use model deployed by C/C++ programmers.

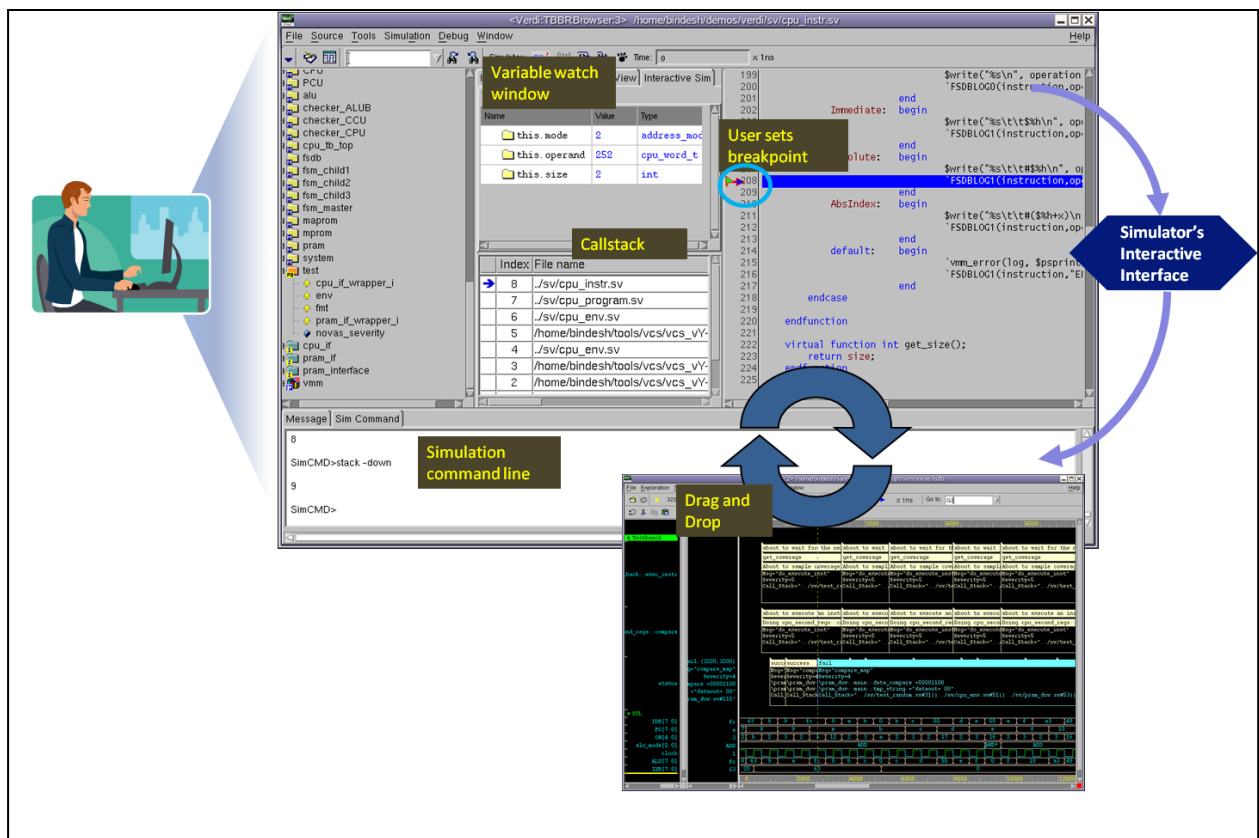


Figure 2: The use of a unified and full-featured debug system to drive interactive testbench simulation can allow for more user friendly set up and visualisation and analysis of results.

There are several compelling advantages of using the debugger to drive the simulator and display its results. Engineers can use the same environment to debug and analyse the behaviour of the design as well as the testbench message logs. Additionally, debug environments provide a more user friendly and familiar environment to drive, view, and analyse the testbench itself. For example, as shown in Figure 2, having variable watch and stack views alongside the source code can greatly enhance the user experience when debugging testbench code.

.... and comprehension

The task of understanding the structure and function of such complex testbenches can be daunting.

Debuggers have always excelled at providing a platform for comprehending HDL source code. Commonly used features, such as design browsing with an instance based hierarchical representation and tracing of loads and drivers, are built upon a knowledge database that is automatically extracted from the source code. While some of this same functionality can be extended to testbench code, the more exciting opportunity lies in building on this knowledge driven foundation to take testbench comprehension even further. Again, many of the ideas proposed here take advantage of practices that have already proven to be successful in the software domain.

Design code is typically built hierarchically with lower level modules instantiated at higher levels and some modules instantiated multiple times. Conceptually, this can be represented in a tree like fashion from the top level module all the way down to the lower level modules. Testbench code however, like C++ and other object oriented languages, is primarily made up of declarations of classes, functions and variables.

During testbench debug and analysis, engineers want a quick way to navigate to a class, function, variable or the newer SystemVerilog constraint and coverage code. Debug and analysis tools have to be able to import this type of code and display a meaningful representation that takes into account the declaration centric nature of testbench code (see Figure 3). This hierarchical representation must also be linked to the actual source code so that when a class, function or other entity is selected, the corresponding source code is also displayed.

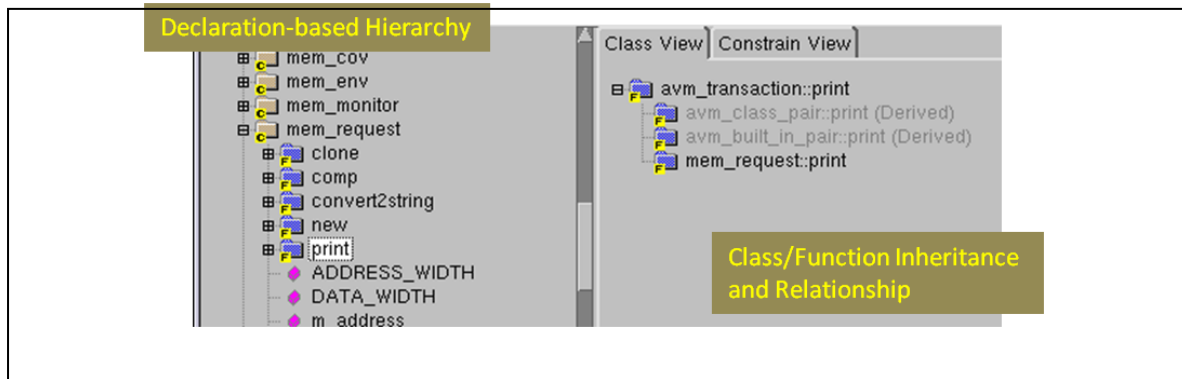


Figure 3: An instance based hierarchy representation and UML like class inheritance and relationship view are critical to SystemVerilog testbench code comprehension.

Given the object oriented nature of SVTB code, engineers can easily reuse existing code and create reusable code themselves. Classes are often derived from existing base or parent classes. This inheritance allows them to retain all the capabilities of the parent while at the same time allowing for variables or functions to be replaced with new ones, or entirely new ones to be added. While declaration based views can be enhanced to show some class hierarchy, most classes have complex relationships with other classes, particularly as engineers understandably take advantage of SVTB 'object orientedness' (or reusability) in its purest sense. To represent this 'organic' nature of classes, the concept of UML class diagrams can be borrowed from the software world.

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