Technology White Paper

# The CHAMP-AV6 VPX-REDI
## Digital Signal Processing Card

Maximizing Performance with Minimal Porting Effort

### Introduction

The Curtiss-Wright Controls Embedded Computing CHAMP-AV6 is a latest-generation, VPX-REDI platform for Digital Signal Processing (DSP) applications. Current users of the Curtiss-Wright Controls CHAMP-AV4 VME-based card undoubtedly are – or will soon be – considering a move to the CHAMP-AV6. This decision is driven by the enormous performance upside of the board itself, coupled with the increasingly acknowledged advantages of the VPX format.

This paper presents information from a benchmark prepared by Gedae Inc. which compares the relative performance of the CHAMP-AV4 and AV6 running a Synthetic Aperture Radar (SAR) application. Also described is the effort required to port an application developed with the Gedae® environment from the CHAMP-AV4 to the AV6.

Figure 1: The VPX format CHAMP-AV6 features four MPC8641 dual processors with SRIO interconnect

### Gedae Development Environment

Gedae, from Gedae Inc., is an Integrated Development Environment that allows engineers to design, test, build and deploy multi-processor DSP applications. The Gedae environment consists of an auto-coding, multi-processor compiler, high-level language, algorithm library, and debug and analysis tools. The compiler takes functional models and hardware architecture and creates an appropriate, multi-threaded application.

Gedae positions itself as a solution to the inherent difficulty in programming multi-core and multi-processor hardware, combined with increasingly complex systems. These two factors can result in fragmented development teams struggling with an equally fragmented, inefficient development process. The Gedae approach allows algorithm developers, as well as system, software and hardware engineers to be directly connected to the product, acting as a unified development team.

Gedae applications are highly abstracted from the underlying hardware. This provides Gedae developers with a high degree of software portability between changing hardware platforms. In the case of this particular benchmark, the porting effort required – as reported by the engineers responsible – certainly confirmed that Gedae greatly simplifies moving advanced multi-processor applications from one generation of hardware to another.

VPX VPX REDI Gedae

Curtiss Wright Controls Embedded Computing



## A Complementary Development Tool

The Gedae software takes advantage of two Curtiss-Wright Controls signal processing software products. The first is Continuum IPC. This is a communications library that provides bulk data transfers and messaging between processors, while providing abstraction from the underlying transport mechanism and DMA facilities. Continuum IPC is offered on both the CHAMP-AV4 and AV6, which in itself is indicative of its hardware abstraction, given the dissimilar architectures of these two cards. Gedae makes use of the best available IPC method, in this case the Continuum IPC components.

Gedae also makes use of Continuum Vector, Curtiss-Wright Controls' DSP function library optimized for AltiVec™. When a customer selects certain signal processing functions in their Gedae application, Gedae will make use of optimized functions from the Continuum Vector library to accelerate the application.

## The Benchmark: Application and Hardware

This benchmark involved the Gedae implementation of a Synthetic Aperture Radar (SAR) algorithm on the Curtiss-Wright Controls CHAMP-AV6 and AV4 multi-processor cards. The polar format SAR algorithm's main computing demand is a 2D FFT. When the 2D FFT is distributed, the algorithm employs a classic multi-processor data movement technique called a "corner turn". It is a known stressor of memory and inter-processor communications hardware, and the time required to perform this data movement can be a key limiter of the overall 2D FFT performance. In a Gedae application, the corner turn is simple and elegant to express. The Gedae compiler handles the complexity of implementation, generating the underlying code involving many local matrix transpositions and DMA transfers, from every processor to every processor. The compiler deals with the complexity, leaving the developer free to deal with application functionality at an abstract level.

The CHAMP-AV4 features a PCI-X ring architecture where each processor is connected to the two adjacent ones via a 100MHz, 64-bit PCI-X bus. The bus has a peak performance of 800MB/s and demonstrates sustained performance under DMA of 570MB/s.

The CHAMP-AV6 employs a Serial RapidIO® (SRIO) architecture. Each processor has a 4-lane SRIO connection to a local IDT (Tundra) Tsi578 SRIO switch. This is a peak 1.25GB/s connection with a demonstrated sustained performance under DMA of 1.0GB/s. The CHAMP-AV6 architecture is non-blocking, permitting simultaneous data transfers between both pairs of processors. The non-blocking nature of SRIO offers more than just a performance advantage for the CHAMP-AV6: it makes it unnecessary to incorporate hardware-dependent data movement techniques (such as ordering and synchronizing) in order to extract optimal performance.

## CHAMP-AV4 Specifications

- 6U VME64x form factor
- Four 1.0GHz Freescale Power Architecture™ MPC7447A Processor with AltiVec
- 32 GFLOPS peak performance
- 256MB DDR SDRAM with ECC per processor
- 100MHz, 64-bit PCI-X "Quadflow" ring architecture
- Two 66MHz, 64-bit PMC mezzanine sites
- Running VxWorks® 5.5

## CHAMP-AV6 Specifications

- 6U VPX form factor
- Four 1.0GHz Freescale Power Architecture MPC8641 Dual-Core Processor with AltiVec
- 64 GFLOPS peak performance
- 512MB DDR2 SDRAM with ECC per processor
- SRIO architecture
- Running VxWorks 6.5


Figure 2: Gedae provides a high-level language capable of expressing algorithms in a compact form. The SAR benchmark is depicted here.

```
out sar(complex src,int C,int R,float taylor[],complex azker[])
{
  int log2C=log(C)/log(2.0);
  Cx=1<<log2C;
  C2=Cx<C?2*Cx:Cx;
  range t;
  range c=C;
  range c2=C2;
  range r=R;
  range rd=R+R;

  /* Generate image */
  r1[c]=src(c);

  /* Range Processing */
  r2[c]=r1[c]*taylor[c];
  r3[c2]=c2<C?r2[c2]:0;
  r4[c2]=dft(r3);
  a1[r][c2]=r4[c2](r);

  /* Transpose and Adjoin */
  a2[c2][r]=a1[r][c2];
  a3[c2][r](t)=a2[c2][r](t-1);
  a4[c2][rd]=rd<#r?a2[c2][rd]:a3[c2][rd-#r];

  /* Azmuth Processing */
  a5[rd](c2)=a4[c2][rd];
  a6[rd]=dft(a5);
  a7[rd]=a6[rd]*azker[rd];
  a8[rd]=idft(a7);
  out[r]=a8[r];
}
```

## Porting Effort

The Gedae tool literally made moving the SAR application from the CHAMP-AV4 to AV6 a few minutes of work. Since Gedae offers mechanisms to express parallelism in the application, changing the number of processors for this particular port was simply a matter of adjusting a variable from four to eight to accommodate the eight processor cores on the CHAMP-AV6. A developer dealing with this change without the benefit of Gedae would expect to spend days to port a well-designed (for scalability) application, or weeks for code that was highly tuned for a specific architecture. More complex applications would demonstrate even greater value.

## Results

The purpose of the benchmark was to determine the real-world performance increase offered by the CHAMP-AV6. At the most simple level, it offers twice the raw floating point performance of the CHAMP-AV4, by virtue of twice the number of AltiVec units on the card. Any computer engineer knows that performance "marketing" numbers are not entirely reliable predictors of system level performance. In real applications, the interaction of processor cores with memory, the latency and throughput of the communications hardware, and the effect of cache size and speed all contribute to the real performance of the machine.

The hypothesis was that the improved memory bandwidth of the MPC8641 processor, and the much faster inter-processor bandwidth afforded by the SRIO architecture, would allow the CHAMP-AV6 to out-perform the AV4 by more than the ratio of the floating point performance.

The SAR algorithm is broken into three main stages:

- Range – FFT and other arithmetic on rows
- Corner Turn – distributed matrix transpose
- Azimuth – FFT, IFFT, and other arithmetic on columns (rows of transpose) of adjoined matrix

The algorithm used a 512 x 2048 image size.

The code was tested on the CHAMP-AV6 using both single-core and dual-core implementations. The VxWorks BSP for the CHAMP-AV6 supports the operation of each core separately (i.e. not SMP). At the Gedae application level each core is equivalent to a separate processor.

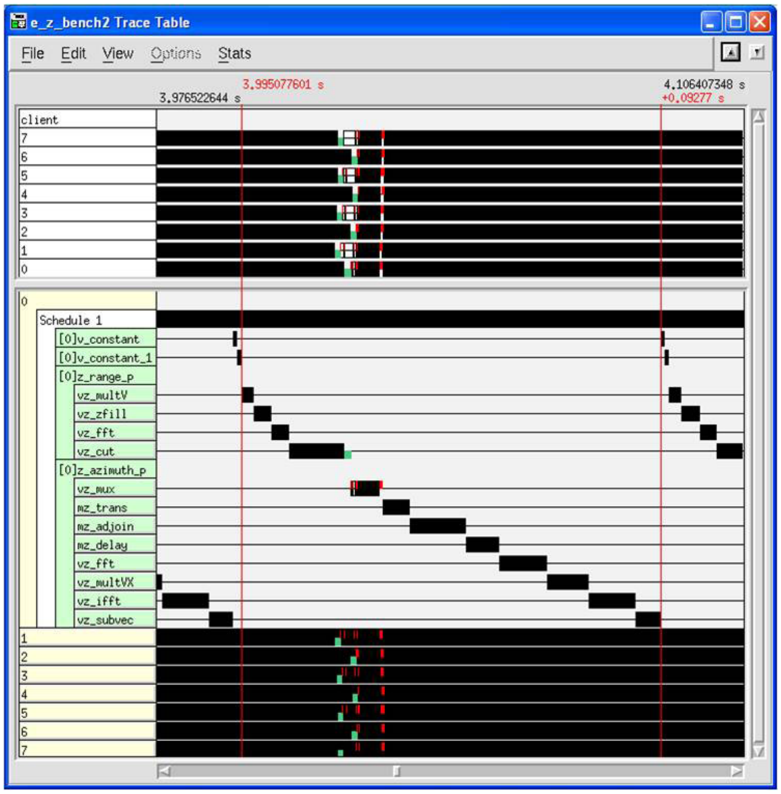
Table 1: Benchmark Results

| Hardware | Number of cores | Time (seconds) | Performance Ratio to CHAMP-AV4 |
|---|---|---|---|
| CHAMP-AV4 | 4 | 0.264 | 1 |
| CHAMP-AV6 | 4 | 0.206 | 1.28 |
| CHAMP-AV6 | 8 | 0.0928 | 2.84 |

The benchmark shows the dual-core CHAMP-AV6 performing 2.84 times faster than the AV4.

The fact that the CHAMP-AV6 outperforms its FLOPS rating relative to the AV4 can be strongly attributed to the inter-processor communication bandwidth of SRIO. There are also performance advantages afforded by the dual-core nature of the MPC8641 where data transfers are occurring in local memory. While the Gedae benchmark test results were based strictly on a card to card comparison, the significant performance upgrade of the CHAMP-AV6 over the AV4 is indicative of a more far-reaching advantage of the VPX module

Figure 3: The Gedae Trace Table tool provides visibility into the real-time execution of the application on the target hardware



format – a state-of-the-art interconnect like SRIO is employed across the backplane as well as within a single card.

The introduction of SRIO means the superior performance of the CHAMP-AV6 on a single card basis is amplified in a multi-card system scenario. In this way a CHAMP-AV6-based DSP system can be made more scalable, as installing additional cards with their attendant processing power will result in a commensurate gain in application performance.

## A Low Barrier to High DSP Performance

The CHAMP-AV6 represents the highest performing multi-processor card in Curtiss-Wright Controls' catalog of COTS products. The Gedae benchmark shows the impressive I/O bandwidth of its eight MPC8641 processor cores. In addition, the data points to the significant performance upgrade of SRIO, which can be leveraged locally and system-wide, thanks to the VPX-REDI format. In this particular benchmark exercise, after an almost trivial porting effort using Gedae, the CHAMP-AV6 is able to display its improved performance numbers on the SAR algorithm.

The Gedae port and benchmarking of the CHAMP-AV6 presents a compelling test case, one that should be considered by DSP system designers wishing to move to this high performance, VPX-REDI platform.