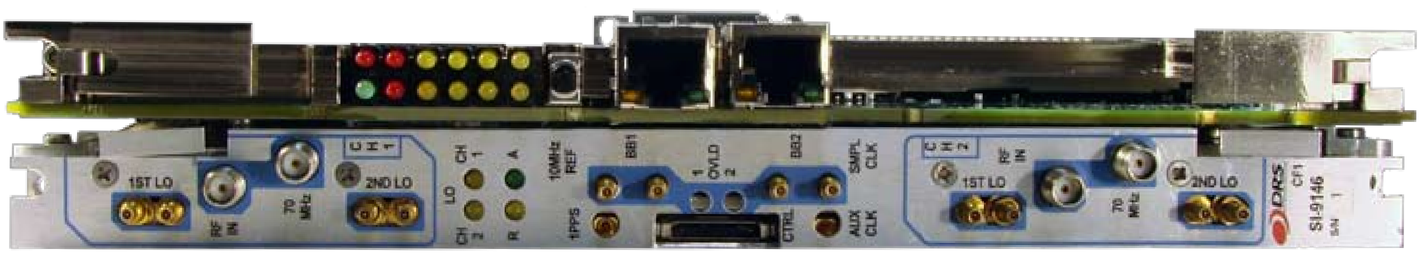
DRS SIGNAL SOLUTIONS, INC.

DRS TECHNOLOGIES

DRS Application Note

Integrated VXS SIGINT Digital Receiver/Processor

Figure 1: DRS Tuner and Curtiss-Wright DSP Engine



Introduction

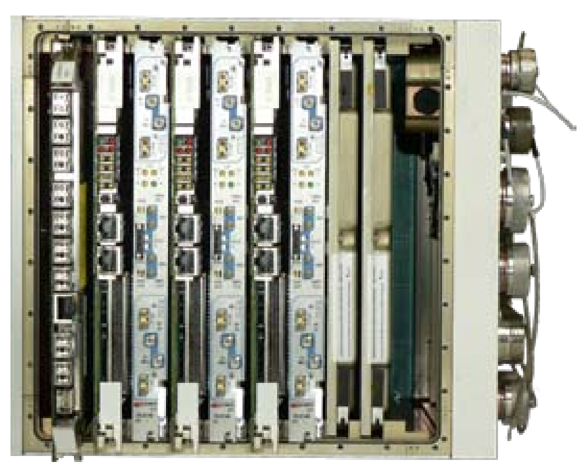
This application note describes a notional Signals Intelligence (SIGINT) solution that can be integrated utilizing a high-performance digital receiver from DRS Signal Solutions and a high-performance Digital Signal Processing (DSP) engine from Curtiss-Wright. The combination of the DRS SI-9146 Dual Tuner and the Curtiss-Wright VPF1 VXS DSP engine presents a low-risk approach to the development of SIGINT and Electronic Warfare (EW) systems for deployment in air-cooled and rugged conduction-cooled environments. System Integrators can reduce their risk and achieve superior performance by basing their design on this proven combination of reliable, high-performance tuner and signal processing hardware that communicate over the high throughput VXS interconnect.

The SI-9146 and VPF1 provide a processing solution capable of processing either two coherent or two independent RF tuners covering a range from 20 to 3000MHz with an instantaneous IF bandwidth of 30MHz for each of the RF channels. Additional channels can be scaled with additional module pairs (SI-9146 and VPF1) added to a VXS chassis.

Modern Transport Technology

Digital tuners are devices that down-convert RF signals from an antenna input to an intermediate frequency (IF) or baseband and deliver the result in digital format. The benefit of having the ADC integrated directly to the tuner is improved signal integrity due to accurate matching of the two stages as well as improved ease of use and reliability due to elimination of cabling between the tuner and digitizer.

Figure 2: ATR chassis with conduction-cooled CSW1, 3x VPF1s and 3x SI-9146s



Digital data representing the quantized IF signal is presented to a signal processor via a digital interface. Early generations of digital tuners supported "wide" parallel data interfaces (16, 32-bits or wider) which required bulky ribbon cables or heavy, expensive, and potentially unreliable backplane overlays.

The advent of multi-gigabit serial data interfaces such as those in modern field programmable gate arrays (FPGAs) provide a more reliable interface that allows the digitized data to be routed either via front-panel fiber-optic or copper interfaces or over a high-performance backplane. Modern FPGAs also support serial protocols such as Xilinx's® Aurora™, serial Front Panel Data Port (sFPDP), or serial RapidIO® (sRIO), providing transport mechanisms for moving data to other FPGAs, to data recording systems, and to multi-processing signal processors.

High Performance VHF/UHF Digital Receiver / Processor System

Although this application note illustrates a notional SIGINT solution, SIGINT solutions based on the Curtiss-Wright VPF1 Signal and Data Processor integrated with the DRS SI-9146 VHF/UHF Digital Tuner have been, and continue to be, integrated and fielded by Curtiss-Wright and DRS customers. BAE Systems has delivered and continues to deliver their Series 3000 SIGINT systems, based on this architecture, to numerous programs in the U.S. Army and U.S. Air Force for operational deployment.

Curtiss-Wright VPF1 Signal & Data Processor

The VPF1 is a high-performance heterogeneous compute engine, supporting a combination of dense FPGA processing nodes (2) and dual PowerPC™ 744x processors. The Xilinx Virtex-II Pro FPGAs provide connectivity to the VXS high-speed serial ports via Multi Gigabit Transceivers (MGTs) routed to the VXS P0 connector. Four (4) MGT lanes each supporting up to 3.125Gbps are routed to each FPGA. The FPGAs support sFPDP, sRIO, or Xilinx Aurora protocols.

Note: In this application, the VPF1 is fitted with oscillators to support MGT operation at 2.5Gbps.

Features:

- 2x PowerPC 7447A CPU nodes
- 2x Xilinx Virtex-II Pro FPGA nodes
- 8x 2.0-3.125Gbit/sec VXS serial communications channels
- Gigabit Ethernet, RS232, RS422, 64-bit, 66MHz PMC site
- VxWorks 5.5.1 & 6.2 BSPs, IP cores for QDR, DDR, PCI, etc.
- Optimized VSIPL DSP libraries, Built-In Test (BIT)
- Air-cooled and rugged conduction-cooled build variants

Figure 3: Curtiss-Wright VPF1, air-cooled version

DRS Technologies SI-9146

The SI-9146 is a VME/VXS, dual-channel, wideband, VHF/UHF tuner that provides independent or phase-coherent down-conversion of RF signals between 20 to 3000MHz. The final IF outputs are 30MHz wide and are sampled at 80MHz by two AD9444 14-bit ADCs. The digital processing section contains two Virtex-II Pro FPGAs as well as FLASH EEPROM which support the development of narrow-band DDC channels and user-defined algorithms. The digital data streams are formatted and output in accordance with the VITA-49/VITA-41 VXS standard. The digital IF output interface is four, high-speed, single-lane, serial ports on the P0 connector. Each lane operates at a transfer rate of either 2.0 or 2.5Gbps, selectable via software.

Features:

- Dual wideband tuner in a single slot 6U VXS card
- 20 to 3000MHz frequency coverage
- 30MHz instantaneous IF bandwidth; 70MHz and 20MHz IF analog outputs
- VITA-9 Digital IF output, with time stamp
- Phase-coherent or independent modes

- Supports LO distribution via daisy-chain (eight channels)
- Tuning speed: 300-microsecond, typical
- Frequency step/sweep scan modes
- Dual 80MHz 14-bit ADCs
- Two Xilinx Virtex-II Pro FPGAs
- VME register-based control interface, front-panel scan control interface
- Cooling options: air-cooled or rugged conduction-cooled

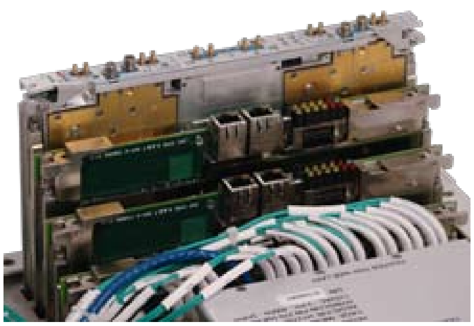
Figure 4: DRS SI-9146 Tuner

Application Overview

The application referenced here is a SIGINT/EW application that illustrates how a system could operate. The following figure shows the hardware layout for a 4-channel SIGINT/EW system. Antennas are connected to the RF inputs of the two SI-9146 digital tuners, each of which provides two digital IF data streams to the VPF1 via a VXS high-speed serial fabric.

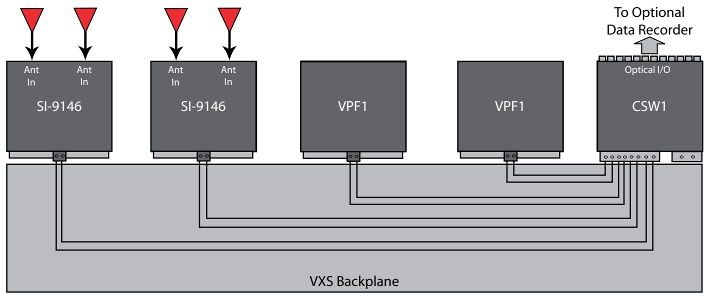
A custom VXS backplane could be used to connect P0 VXS links of the SI-9146 and VPF1 boards directly, but in this application the data would be routed through a VXS switch such as Curtiss-Wright's CSW1 to allow the use of a standard VXS backplane for application flexibility and growth to support additional system capabilities. With the CSW1 the data streams can be multicast out the front panel of the CSW1 to support simultaneous high-speed data recording.

Figure 5: Front panel connectivity



The SI-9146 down-converts antenna signals at RF carrier frequencies to an intermediate frequency and digitizes the IF signal. The SI-9146 encodes the digitized wideband signal data and current tuner settings in VITA-49 packets[1] and transmits them across the VXS links (high-speed serial links on the VXS P0 connector) using the Aurora transport. Each channel creates data at a rate of 160MB/s.

Figure 6: Hardware layout of a 4-channel SIGINT/EW system



As many as eight tuner channels (4x SI-9146's) can be used in phase-coherent mode by daisy-chaining the LOs (no LO distribution module needed). Additionally, the SI-9146 provides sufficient resources in the on-board FPGA to support custom user-defined pre-processing of the ADC sampled data.

The VPF1 processors support VxWorks® 5.5, 6.2 or Linux® (2.6 Kernel). In this example, the processors would boot the O/S and execute an application. The application controls all elements of the VPF1, from configuring the FPGAs and providing specific parameters within the FPGAs, to performing Digital Signal Processing (DSP) on data transferred from the FPGAs to the processors.

During initialization of the application, the FPGAs on the VPF1 would be configured and held in reset until the tuners are configured. The SI-9146s can be configured and initialized via VME from one of the VPF1 boards. Attenuation, gain, tuning frequencies, etc. would be set during this initialization. Once configured, the operational program would begin the process of accepting data from the tuners.

Digital Signal Processing

The VPF1 "slice" architecture of tightly coupled FPGA and PowerPC processor is ideally suited for SIGINT and EW processing applications. This architecture allows for efficient processing of incoming digital tuner data streams in parallel.

Figure 7: VPF1 "slice" architecture block diagram

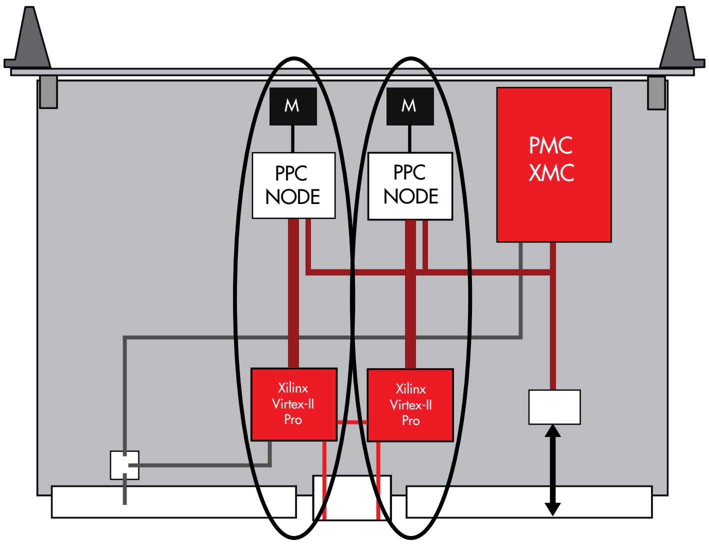
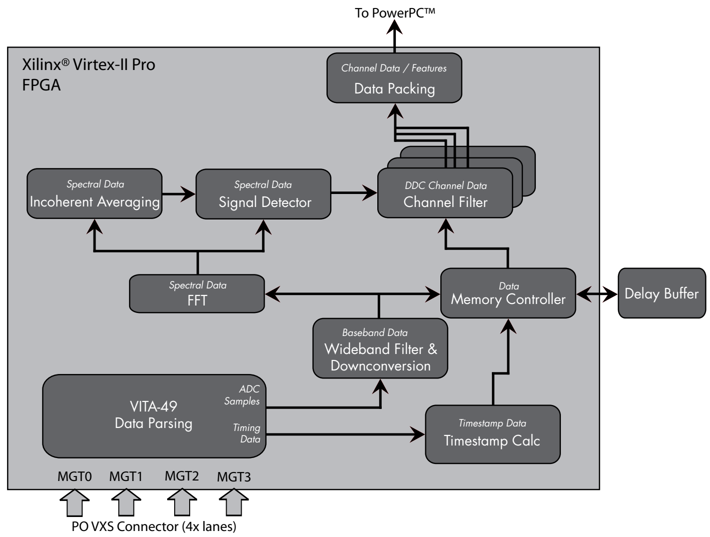


Figure 8: Xilinx Virtex-II Pro FPGA processing flow



VITA-49 format data streams from the tuners are initially processed in FPGAs on the VPF1. The FPGA processing is designed to provide signal detection, digital down-conversion (DDC), and extract specific signal parameters for use by the signal processing software running in the PowerPC's. The FPGAs are ideal for high performance parallel processing required to perform the signal detection and DDC functions.

The following example shows how data from the SI-9146 tuner can be processed in the VPF1 FPGAs:

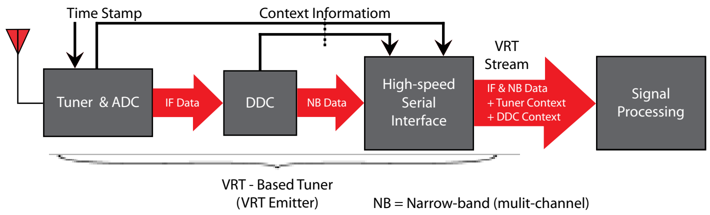
- FFT
- Incoherent averaging to determine approximate noise floor and detection thresholds
- Signal detection
- Digital down-conversion (DDC) and channel processing
- Channel feature extraction and timing reference correlation

Individual narrow-band channels are then forwarded from the FPGA to the PowerPC Processor for additional processing. This processing could also include further channel-specific feature extraction. When operated in phase-coherent mode, beam-forming, direction-finding, or geolocation processing can be performed.

VITA-49 Data

The VITA-49 standard is commonly referred to as the VITA Radio Transport (VRT). The VRT specification defines a transport-layer protocol designed to allow digitized radio signals and related information to be conveyed from one system or module to another. The primary application of VRT is for the packetized transport of time-domain samples of RF, IF, or baseband signals along with relevant metadata via a digital interface.

Figure 9: Example of a system implementing the VRT protocol



The tuner down-converts an antenna signal at a carrier frequency to a wideband, baseband intermediate frequency (IF), digitizes it, and passes it to a digital down converter (DDC) section. Tuner context is composed of such information as the antenna location (GPS), tuned frequency, attenuation setting, time stamp, sample rate, ADC overload status.

The DDC section provides one or more digital tuners that can be tuned to any frequency in the wideband data stream. It also narrows the bandwidth to values useful for typical communication signals. The DDC context consists of such things as tuned frequency and bandwidth.

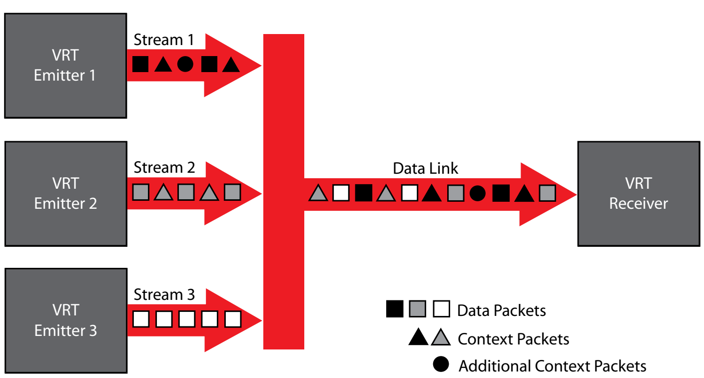
The high-speed serial (HSS) interface collects the data and context information, encodes it according to the VRT definition, and outputs it as a VRT stream.

VRT supports the transport of four types of information: IF data, IF context, extension data, and extension context. VRT defines rules controlling the structure and function of packets that carry these four types of information. It also specifies a way to associate the different packet streams that carry the different portions of the information related to a signal or set of related signals.

In the VRT specification a transmitted sequence of packets that conveys one portion of this information is referred to as a VRT packet stream, or when the meaning is clear, simply as a packet stream. The collection of VRT packet streams needed to convey all the required information about a signal, or signals, is referred to as a VRT information stream, or simply as an information stream.

Systems that output VRT streams are called VRT emitters. Systems that receive VRT streams are called VRT receivers.

Figure 10: VRT emitters and receivers



In this example, each emitter outputs one VRT information stream. Each information stream consists of one or more VRT packet streams and each of these packet streams conveys some portion of the total information to be conveyed about a signal. The figure above depicts each packet stream by a string of identical shapes, each of which represents a packet. The shape of each packet is related to the kind of information it carries. Square packets carry IF data and triangular and round packets carry context. Each packet's color (white, black, or grey) indicates to which information stream it belongs.

The first emitter outputs three packet streams, one for IF data and two for context. Each context packet stream conveys some portion of the required context. For example, the first might convey GPS information while the second conveys the model and serial numbers of installed modules. VRT supports putting any number of context packet streams into an information stream. Only one data packet stream is allowed in an information stream however.

Summary

The combination of DRS Signal Solutions Digital Tuners such as the SI-9146 and Curtiss-Wright Signal Processing Engines such as VPF1 (and VPF2) form the foundation of reliable, high-performance, multi-channel SIGINT and EW digital receiver/processors solutions. Real-time signal detection, identification, direction finding, and geolocation are just a few of the solutions that are now possible with this proven technology.

A discussion of theoretical applications can be useful, but real-world applications are the proof points that customers want to see. There are a number of customer integrated, deployed, field-proven SIGINT applications based on the combination of the SI-9146 and VPF1 VXS architecture such as the Series 3000 SIGINT systems that BAE Systems has delivered for operational deployment in numerous U.S. Army and Air Force programs.

A SIGINT system based on the SI-9146 and the VPF1 requires application specific development to integrate the SI-9146 and the VPF1. This integration effort can be taken on by the customer or contact Curtiss-Wright for a proposal based on your requirements. For more information on the DRS Signal Solutions digital tuners and Curtiss-Wright DSP platforms, how they are integrated, and how you can leverage this integrated solution in your next generation SIGINT application, contact your DRS or Curtiss-Wright sales representative.

Contact Information

To find your appropriate sales representative, please visit:

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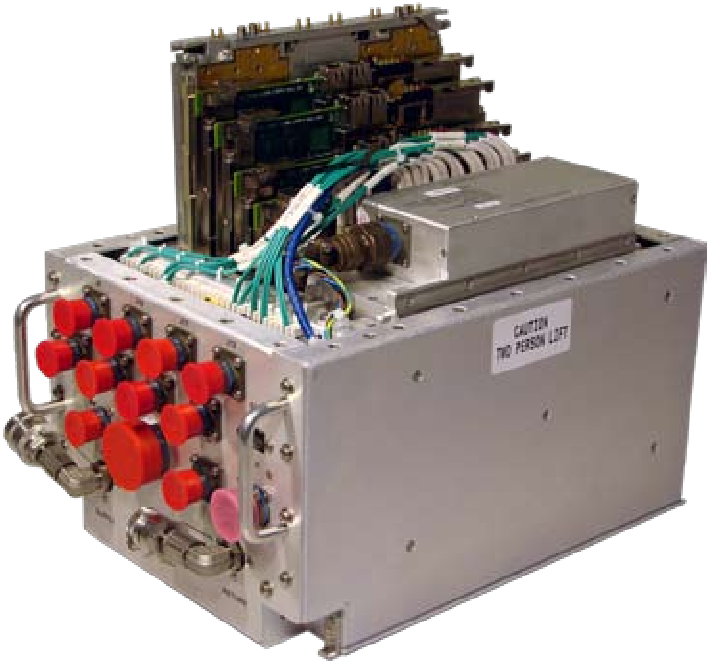
Figure 11: SIGINT/EW System



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