

DDS design suits deep

A low power direct digital synthesiser design has application to deep submicron processes. By **Peter Saul** and **Andrew Saul**.

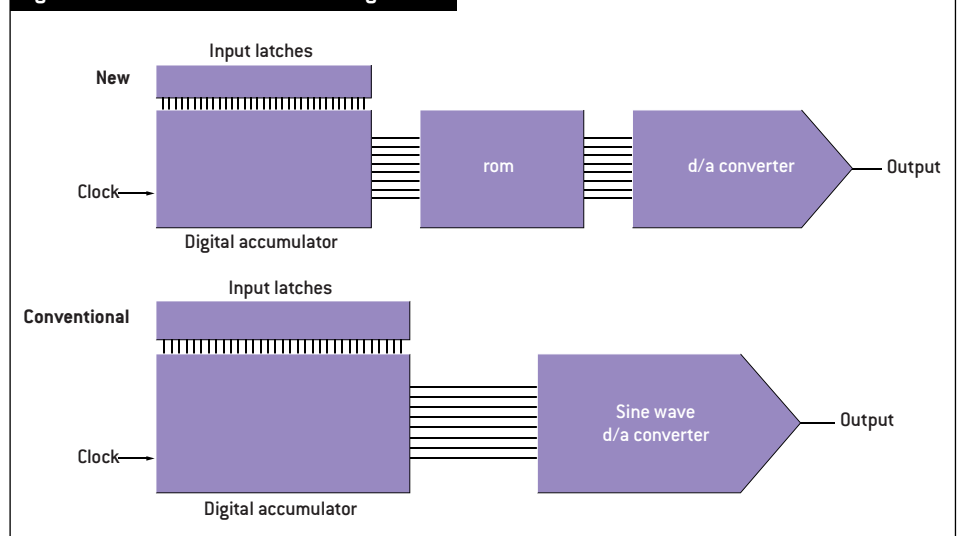
The direct digital synthesis (DDS) principle was described at least 30 years ago [1]. The standard configuration [see figure 1], still dominant today, uses a digital accumulator, a rom to convert the accumulator output to a digital representation of a cosine wave, and a d/a converter to convert the rom output to analogue form, typically for use as the local oscillator in a receiver or transmitter.

The weaknesses of this configuration are in the rom, where access time is critical, and in the d/a converter, where access time can be an issue and accuracy is critical. However, a solution can be found to both of these problems and it brings the added benefits of power reduction, speed enhancement and an approach to accuracy that may be exploited on smaller geometry processes.

The DDS is simultaneously capable of high clock frequencies (in excess of 400MHz) and low power consumption (less than 30mW). A demonstrator chip, created on a 0.35 μ m technology, has proved the basic concept and shown the design is

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Fig 1: Conventional and new DDS arrangements



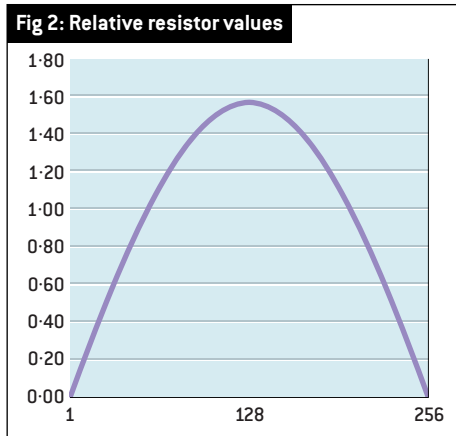
applicable to other silicon processes, especially those where accuracy is a limiting issue, such as deep submicron technologies.

A recent paper [2] showed a d/a converter based on 'resistor ladder' principles. Although the earliest d/a converters used this approach, it has been, for the most part, neglected, as it has been perceived to be too slow for many applications. In [2], speed was not an issue, but power consumption was, so the resistor ladder was fed by a 100nA current and this constituted the bulk of the current consumption. Although only an 8bit device, the bit size was 400 μ V, a very low figure for a static d/a converter and compatible with 12bit operation when using the full supply voltage of 3.3V. This was confirmed by measurements on the samples.

The simplicity of that d/a converter structure lent itself not only to accuracy, but also deliberate d/a converter non linearity to a cosinusoidal response. Thus, the DDS need not have a rom at all, but the rom function was included in the d/a converter function [see figure 1].

The d/a converter used the resistor ladder approach, with a cosinusoidal set of resistor values. For the 8bit device of the demonstrator, a total of 256 resistors was used, including the values 0 and 255. As in the case of the linear d/a converter, each individual resistor value was required only to be within $\pm 50\%$ of its nominal value to achieve differential accuracy to the full ± 0.5 LSB specification. Even this somewhat overstates the requirement; the resistors needed only to be within $\pm 50\%$ of the local average value of the resistivity for the achievement of differential accuracy.

In the main resistor chains, this was easily achieved. Some care was needed at the ends of the chains, as, in the configuration used, the chain was continued between blocks in metallisation and this was required to be substantially less than 0.5LSB. Since all levels were ratio dependent, temperature coefficients of resistivity were unimportant for the resistors and only marginally so for the metals. The d/a converter was designed for 100mV analogue output range, buffered on chip to 2V, so the bit



size was equivalent to more than 12bits accuracy in a full scale design. The chip was realised on a 0.35µm process, where resistor absolute accuracy was approximately 12% and matching, for the resistor dimensions chosen, was better than 0.2%. The resistor dimensions were therefore chosen, not for accuracy in the resistors themselves, but for tolerance of the metal interconnect. In the DDS configuration, integral linearity was important to assure low spurious output levels. No segmentation was used to achieve full accuracy.

The full ratiometric accuracy was not practical at the lowest values, but assessment of the error involved at these locations showed such accuracy was not important around the limits of the output, where bit size was very small. The main accuracy requirement was at the centre.

The requirement for the accumulator was to add the contents of a frequency setting register to the sum register and to retime the outputs. This was achieved using standard logic blocks, laid out for minimum chip area.

The d/a converter layout consisted mainly of digital blocks, with each bit consisting of a 4x inverter gate cell reconfigured to act as an analogue switch. Thus the array consisted of 256 cells, each having X and Y control inputs: the resistor for the bit location in the chain and a segment of the voltage output line. The addressing, for 8bits, consisted of two 4 line to 16 line converters, feeding the X and Y address lines.

The ladder to ladder metal straps were within the size of 1LSB, so were not end corrected; this might be a useful option for a system aimed at very high speed or accuracy of more than 14bit.

The DDS included the accumulator described above, again realised in standard digital library cells. The whole of the DDS was extracted and

resimulated to confirm layout accuracy and operating speed. The extraction included vertical parasitic capacitances on tracks, but not lateral terms, so was slightly optimistic; the real chip results are more relevant in this respect. Operation at 400MHz was demonstrated, with some loss of accuracy due to slew rate limitations. The worst case spurs were greater than the expected -49.6dB, but by less than 1bit. Operation at 500MHz showed further degradation. The operating limit was the total capacitance of the voltage output line, which acted as a load for the single switch in operation at any instant, and which was fed in turn by the resistor ladder. It was unfortunate, but unavoidable, that the greatest error from this source occurred at the centre of the output range and thus generated the worst spurs.

This article has described a DDS concept using a combined rom-d/a converter approach. The d/a converter was based on long established principles, but avoided many of the problems of such structures by minimal capacitive loading of the output line. In operation, the dominant current term was the resistor ladder current, typically set at 8mA, for a total current in the DDS at 3V supply of 10 to 16mA, code and clock frequency dependent. On chip buffering minimised loading of the output node. DDS operation to more than 100MHz output frequency and 500MHz clock was possible. Under reduced supply conditions, total current was less than 8mA at 2V and operation at 25MHz output was possible.

For comparison, commercial parts (3) use 180mA at 5V, almost 20x the power, albeit for a more complex device. The accuracy demands of the design were minimal, while the speed was primarily determined by the loading capacitance of the output node. As process geometries are reduced, speed of operation will increase without compromise in accuracy. The design was based almost entirely on standard library cells, so transport of the design would be relatively easy. Resistor values were calculated automatically, but laid out manually; so it should be possible to further automate the design process.

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References

1. V. Manassewitsch, "Frequency Synthesizers Theory and Design", John Wiley, Third Edition 1987, ISBN 0-471-01116-9, p37 et.seq., (First edition 1976).
2. P.H. Saul, A.P.Saul "Nano Power DAC with 400 Microvolt Bit size in a CMOS 0.35um Process", ASP 2006, Oxford Brookes University, ISBN 1-873640-42-0 pp 12-1 to 12-5.
3. Analog Devices Data Sheet, AD9959, released July 2008.

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