Digital Direct Up-Conversion

- the ultimate step for precise RF-generation –

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Pre-Face, traditional RF generation with analog mixers

In modern RF systems the generation of the final signals is usually made in several steps.

Most common, the base-band signal is produced with dedicated digital logic, using FIR-filters, NCOs and complex multipliers technologies. The digital logic is located either in FPGAs or ASICs.

With today's technology, the RF generation in the digital portion is usually limited to appx. 100 MHz and mostly a signal in the range of 28..50MHz is generated.

Because this is usually not the final band, further operations with the intermediate signal (IF) must be performed.

If only a fixed final frequency is desired, the IF signal will easily be multiplied with another fixed frequency and applied to a band-pass, which eliminates the inherent mirror image.

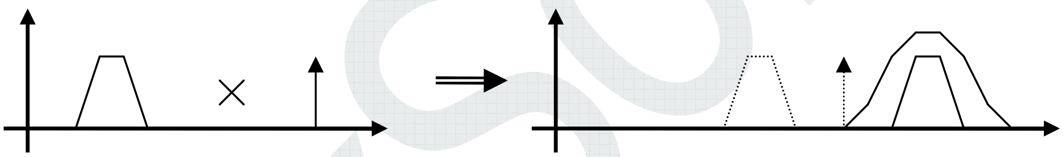

Figure 1 : Shifting up an IF signal to the (fixed) desired band

More complications arise when the final signal must be tunable. This is e.g. the case for CATV modulators, where the RF-generation must take place in a typical range of 100..900 MHz.
A simple frequency multiplier can't be used, because such a solution would require precise tunable bandpass filters.
Instead, the IF signal is multiplied and band-passed into a much higher frequency band (e.g. 2.5 GHz). After this, the signal is downshifted with another tunable multiplier into the final TV band.
We cannot get rid off mirror images, but after the last stage the mirrors are located far away from the final signal and can easily be eliminated with low-pass filters.

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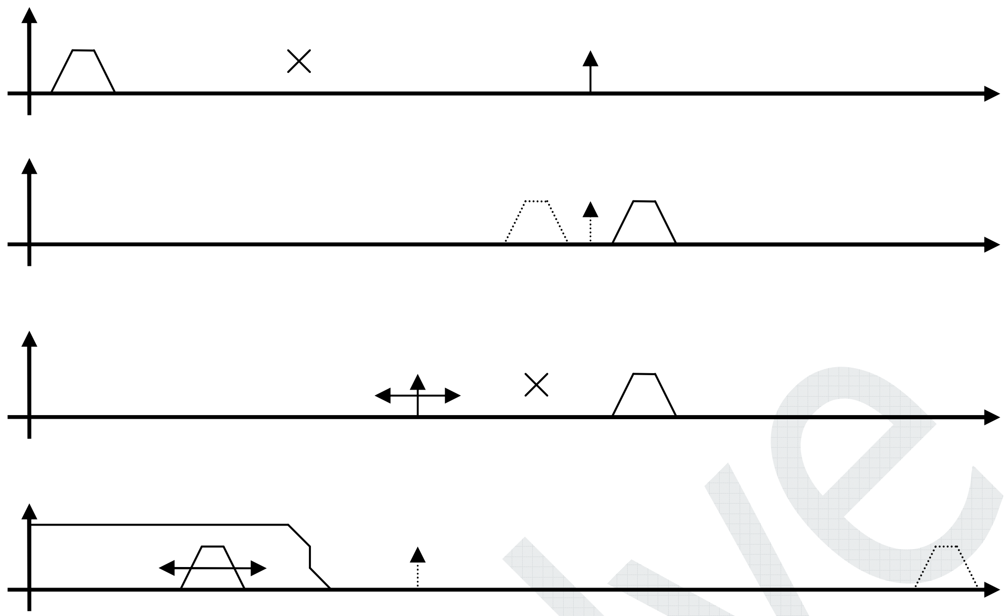

Figure 2 : Shifting up and down an IF signal to a variable desired band

The above described method of RF generation is realized (in various flavours) in CATV head.-ends, cellular base-stations and other professional equipment. The method is proven, is fairly stable and good.
But … it is not good enough!

First, we encounter the usage of at least three oscillators in the system. One for the IF-generation, one for the first mixer and one of the final mixer.
Oscillators have jitter, which deteriorates the signal quality significantly. And the bad news is, that once jitter is induced in a system, it is nearly impossible to remove it.
The 3-stage frequency multiplication not only adds the jitters of the oscillators, but any signal multiplier increases the jitter by factors.
This means, a traditional up-converter requires exceptionally good oscillators.

Second, we need at least one band-pass filter after the IF is transferred to the high-frequency domain. Although such filters only consist of coils and capacitors, the quality of these components must be very high (i.e. low tolerance).
A real filter is not flat in the pass-band and does not have infinite attenuation in the stop-band.
With this, we will have filter unbalances and residuals of unwanted mirror images which decrease the overall signal quality.

Last but not least, the used components for 3-stage up-conversion seem to be cheap if we only have a look to the BOM of the system.
But, we have a high number of passive components and manufacturing and testing of such circuits is complicated, time-consuming and expensive.

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Also the natural aging of passive components must be kept in mind. It's hard to warrant an unchanging quality of the overall system over a longer period of time.

All in all, the traditional method of frequency agile RF-generation has a vast number of disadvantages and replacement with newer approaches is mandatory for future designs.

Digital Direct Up-Conversion using modern FPGAs and DACs

Recently at least two manufacturers of high quality analog components started mass-production of DACs with sampling rates above 2400MHz. With such units, the direct generation of RF-signals up to 1GHz is possible with few additional analog components.
In marching step with these new digital-analog converters the leading FPGA manufacturers have recently introduced logic arrays which can handle the tremendous data rates required to feed such converters.
A 2400 GSps DAC (such as Analog Devices AD 9739) has 28 data lines with 1200Mbps each and a Stratix-III or Stratix-iV has enough I/O bandwidth to handle extremely high data rates.
The built in SERDES-channels make it easy to generate the high speed data, while internally operating at a fractional of the LVDS data rate.

At 2400GSps an internal operating frequency of 300MHz is a good choice, where the modern FPGAs can even handle complex calculations without running into any setup/hold problems. Most of the adders/multipliers have an fmax above 550..700MHz and 300MHz are in a range where the device never will be over-stressed.

Mixing I/Q directly at the final frequency with a numerical oscillator produces a nearly spurious free final signal quality and only a simple analog low-pass filter after the DAC is required to eliminate the mirror images resulting from the DAC sampling frequency.

The usage of NCOs has the advantage, that a signal can be generated with an accuracy of better then +/- 1Hz, and only the sample rate oscillator is critical regarding jitter performance. This oscillator operates at a fixed frequency (e.g. 2400MHz) , which even makes the job easier.

The biggest problem in the up-conversion chain is the fact, that the final stages of the digital filters must be capable of generating multiple samples per clock. And also, the NCOs which run at a lower rate (e.g. 300MHz) must be able to generate a bunch of phase shifted sine- and cosine-samples at one clock period.

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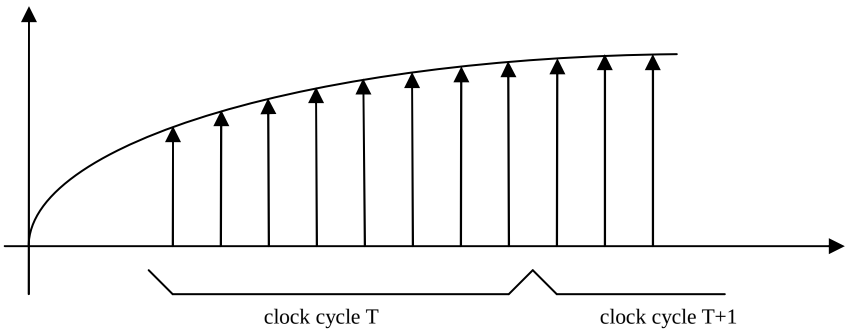

Figure 3 : Generation of 8 NCO samples per clock cycle

With Stratix-FPGAs this is not a problem, because such FPGAs have enough internal resources to do the job in a great way. Especially the DSP-units, which perform pipelined multiply-accumulates at highest throughput, are important building blocks in the final stages of the digital chain.

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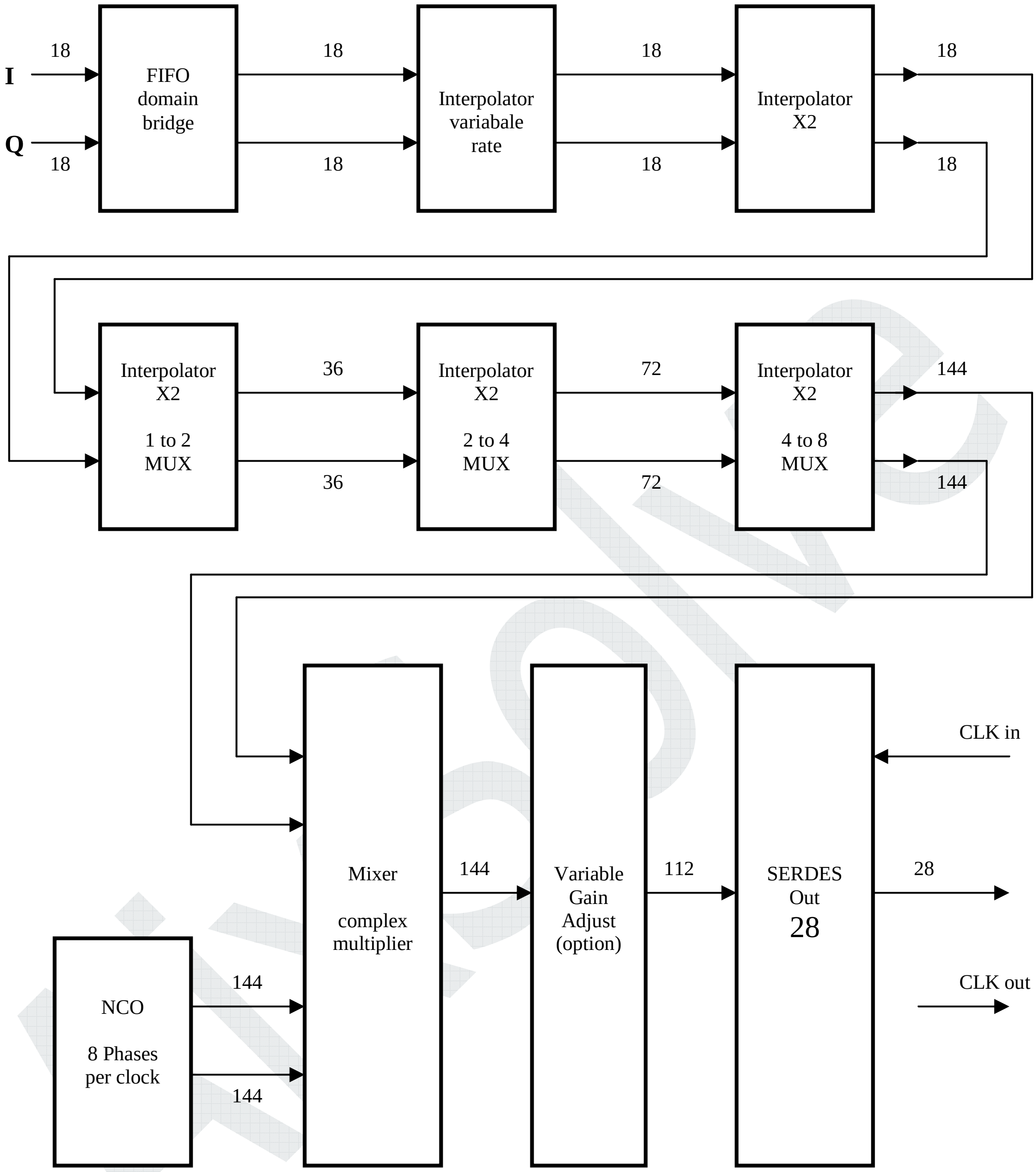

Figure 4 : Typical data flow, direct digital upconverter

A great advantage of digital signal generation is the fact, that once a modulator/up-converter is constructed and tested, a multi-channel system can be derived by simply instantiating (i.e. copying) additional channels.
The output signals of the channels must only be added and a multi-channel up-converter is ready-for-use.
The only limitation factor for generating a plurality of RF-signals is the bit-depth of the selected AD-converter.

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With a 14-bit AD-converter – as used in the sample application – a set of up to eight QAM-carriers is a good number, if the requirements of most CATV-providers should be met.
ACRs in the area of 50dB and MERs in the area of 46dB are possible with using a mid-range Stratix FPGA.

The sample application with eight QAM modulators fits into a Stratix-IV-GX FPGA of class 110 and uses an AD 9739 RF-DAC.
All modulators are independent regarding carrier frequency and symbol rate. This means, that each of the 8 channels can be located anywhere in the CATV band. And each of the 8 channels may have it's own symbol rate.
There are even FPGA resources left, so that a user is able to add code for interfacing the up-converter/mixer with the transport stream sources.

The up-converter cell is not only limited to generate QAM-signals, but can easily be used to generate COFDM and QPSK signals.
As long as the nature of the base-band is IQ, the up-converter building block will transfer the signals to the desired frequency band.

RF up-conversion in the all-digital way with modern FPGAs and DACs is the technology of the future.
The solution enables CATV head-end manufacturers to build EDGE-QAM generators with high quality, low component count, low power and excellent manufacturability.

The up-converter block is soon available as a time-limited cell and can be bought in the encrypted format, with all necessary documentation.
The VHDL-based source of the up-converter/mixer is also available on request.

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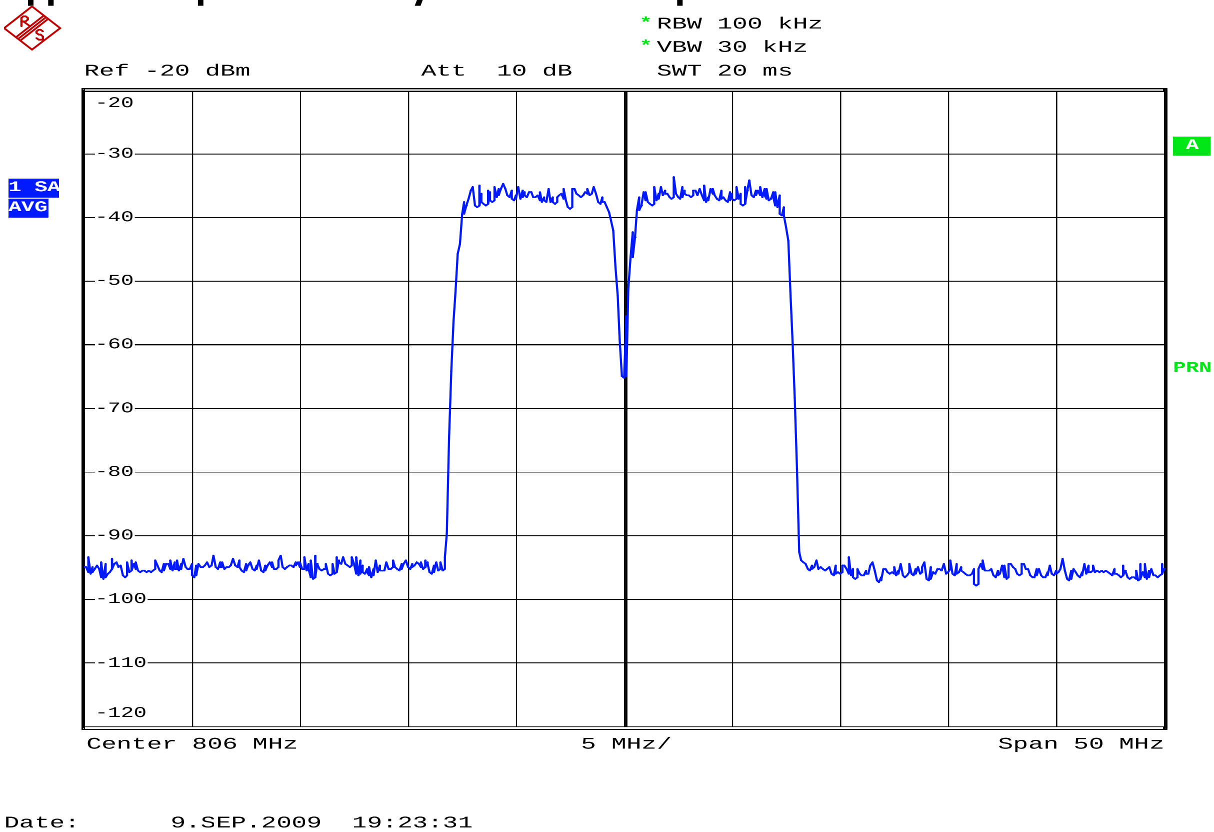
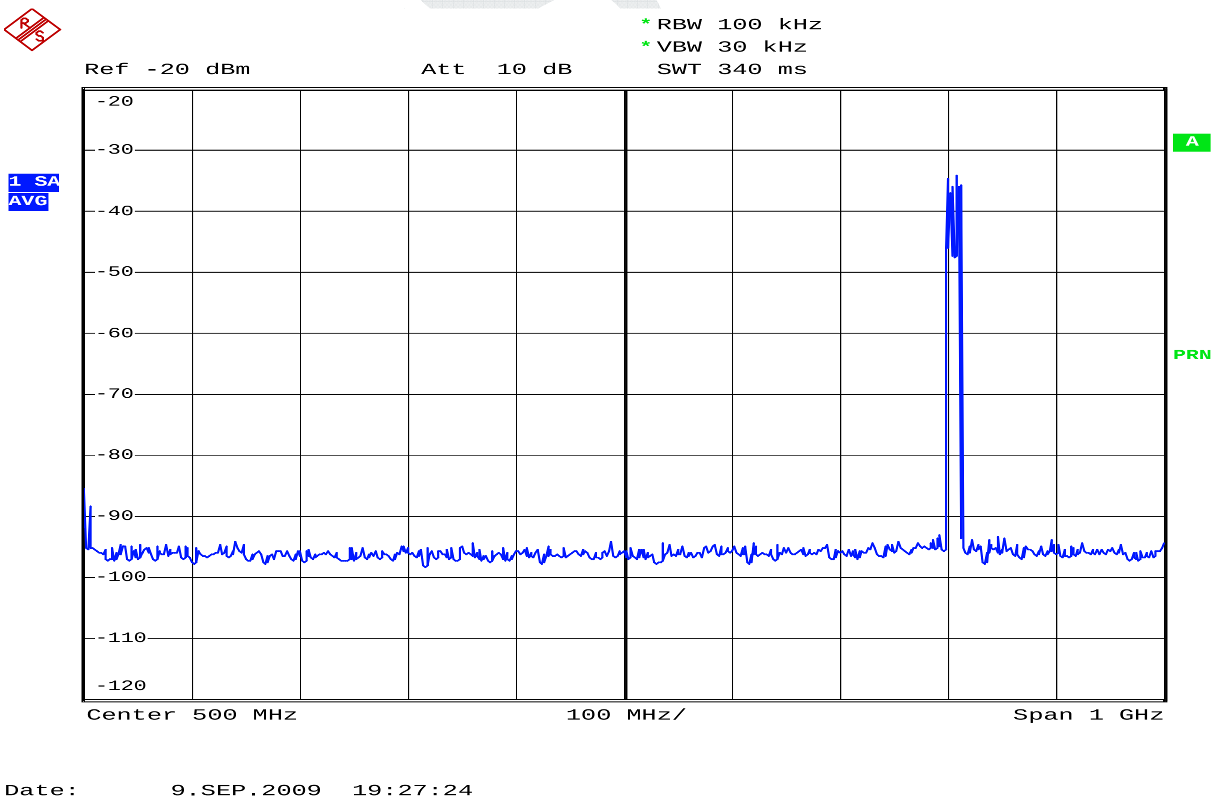
Appendix: Spectrum Analyzer screen dumps



Screen 1a : 2 channel QAM, 6900MSps, 8MHz channel raster, 802MHz ff



Screen 1b : 2 channel QAM, 6900MSps, 8MHz channel raster, 802MHz ff, full band

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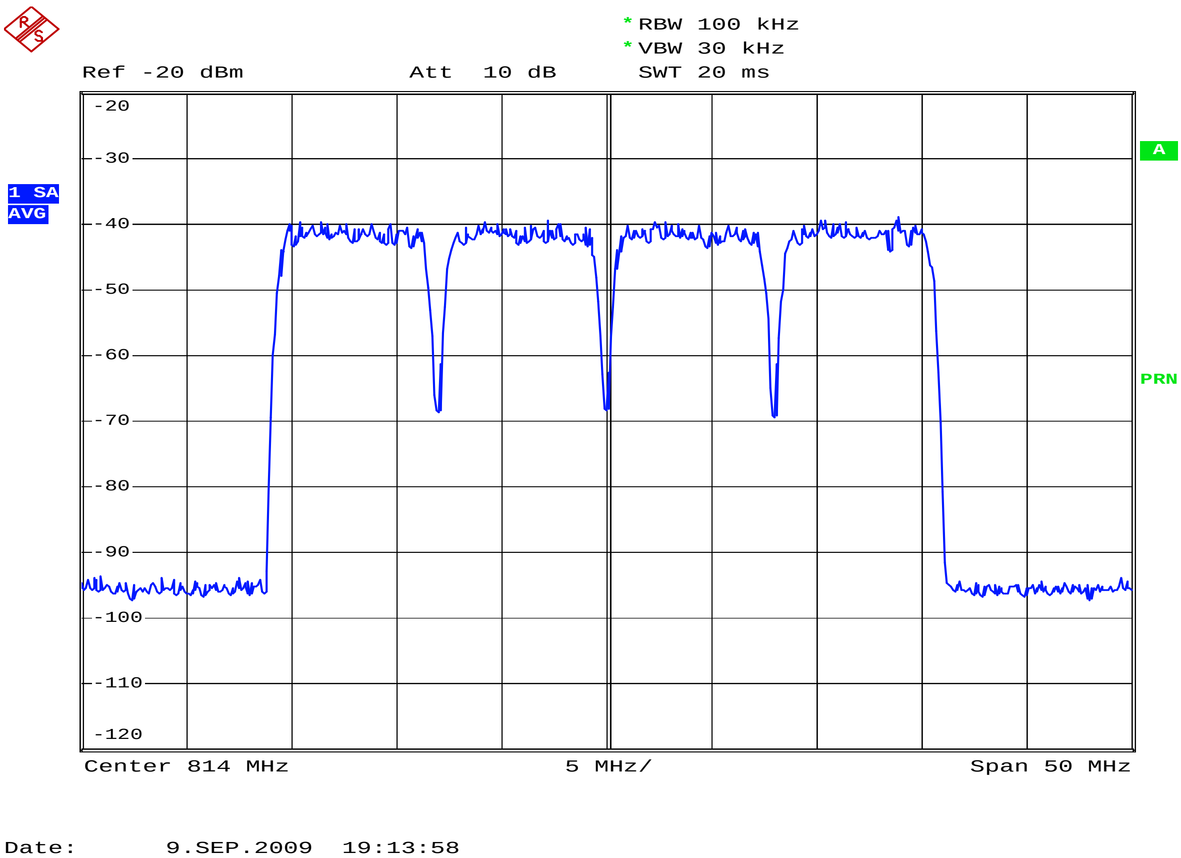
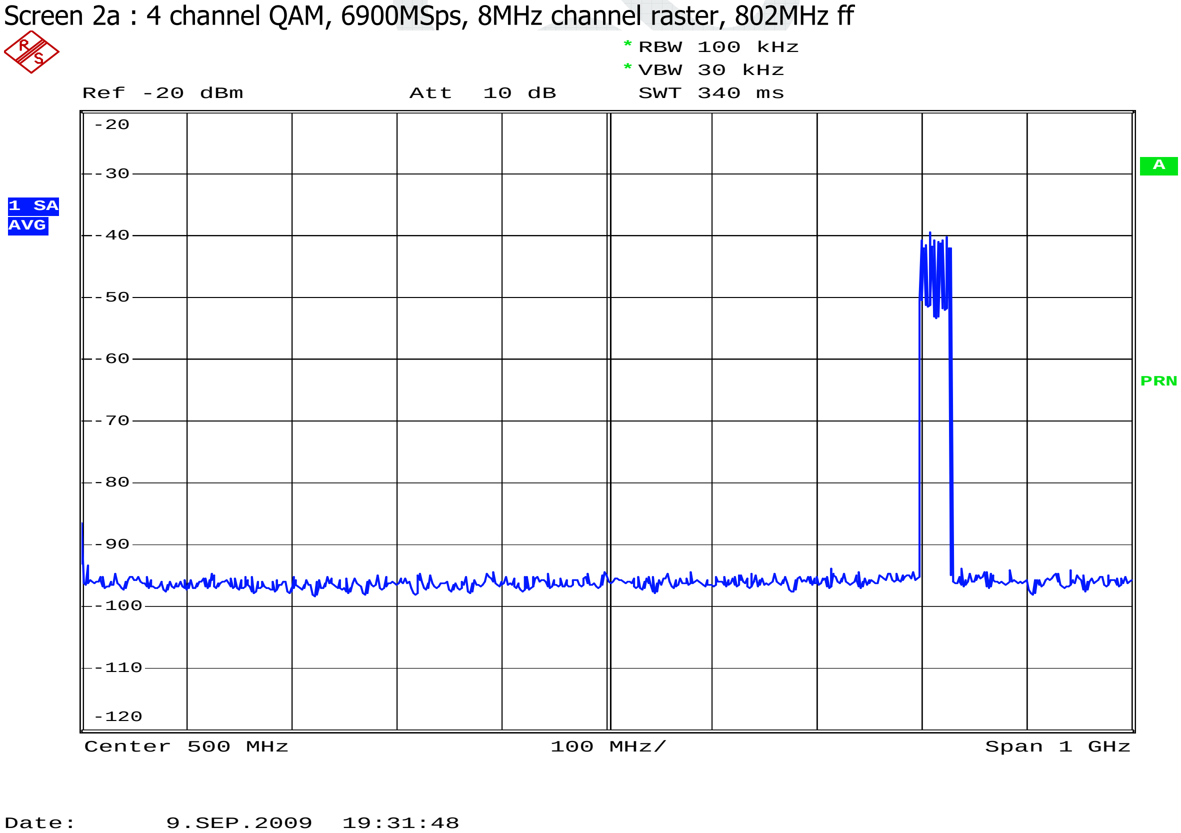


Screen 2a : 4 channel QAM, 6900MSps, 8MHz channel raster, 802MHz ff



Screen 2b : 4 channel QAM, 6900MSps, 8MHz channel raster, 802MHz ff, full band

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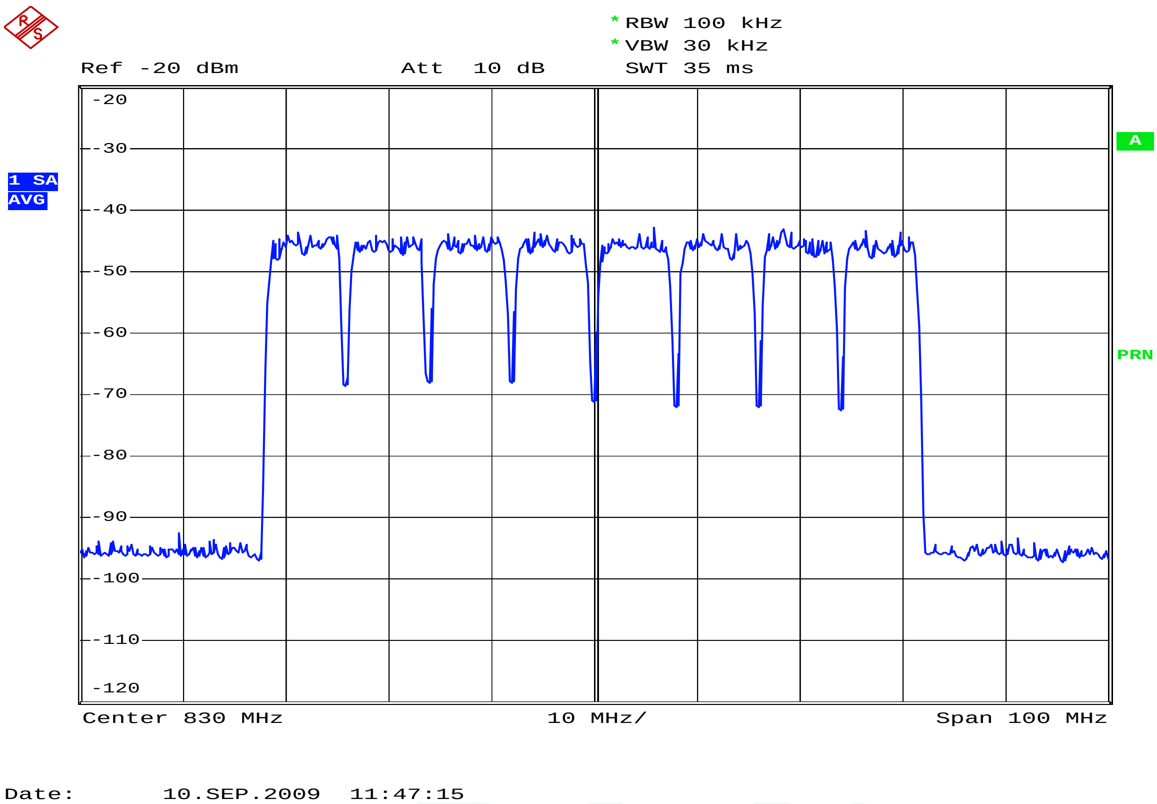
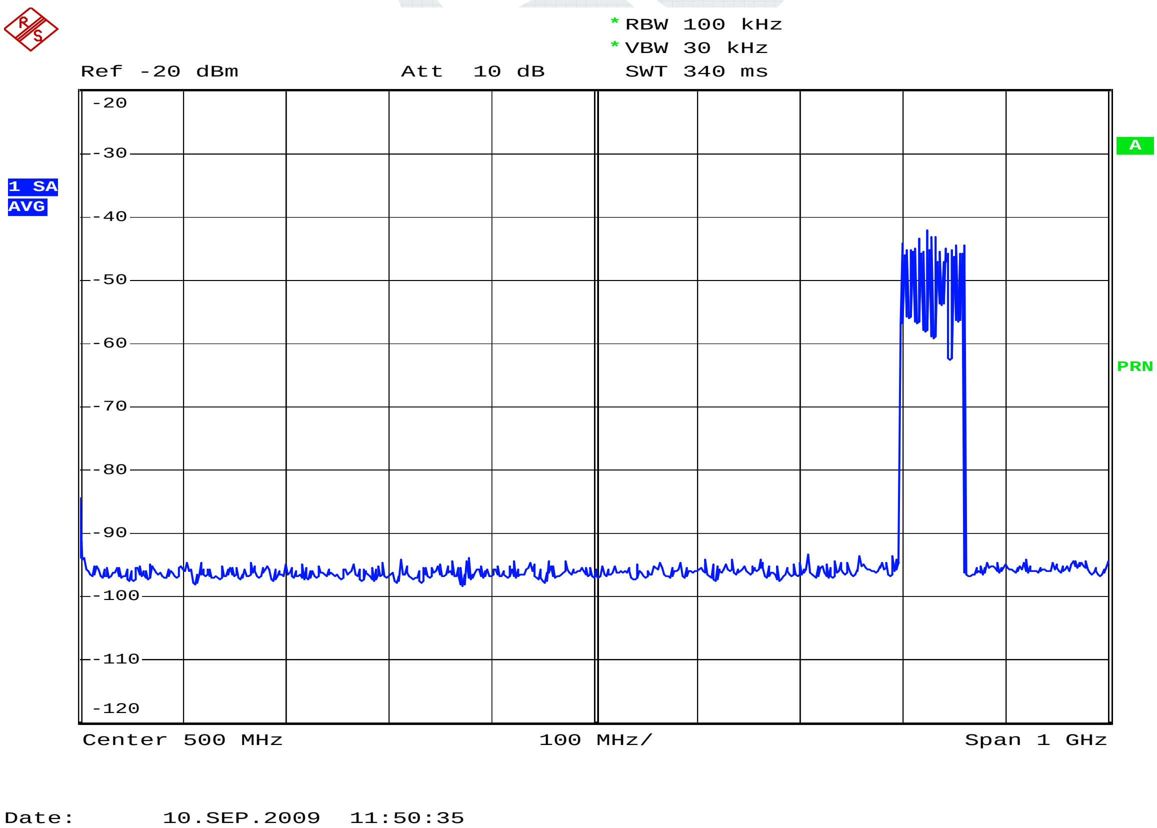


Screen 3a : 8 channel QAM, 6900MSps, 8MHz channel raster, 802MHz ff



Screen 3b : 8 channel QAM, 6900MSps, 8MHz channel raster, 802MHz ff, full band

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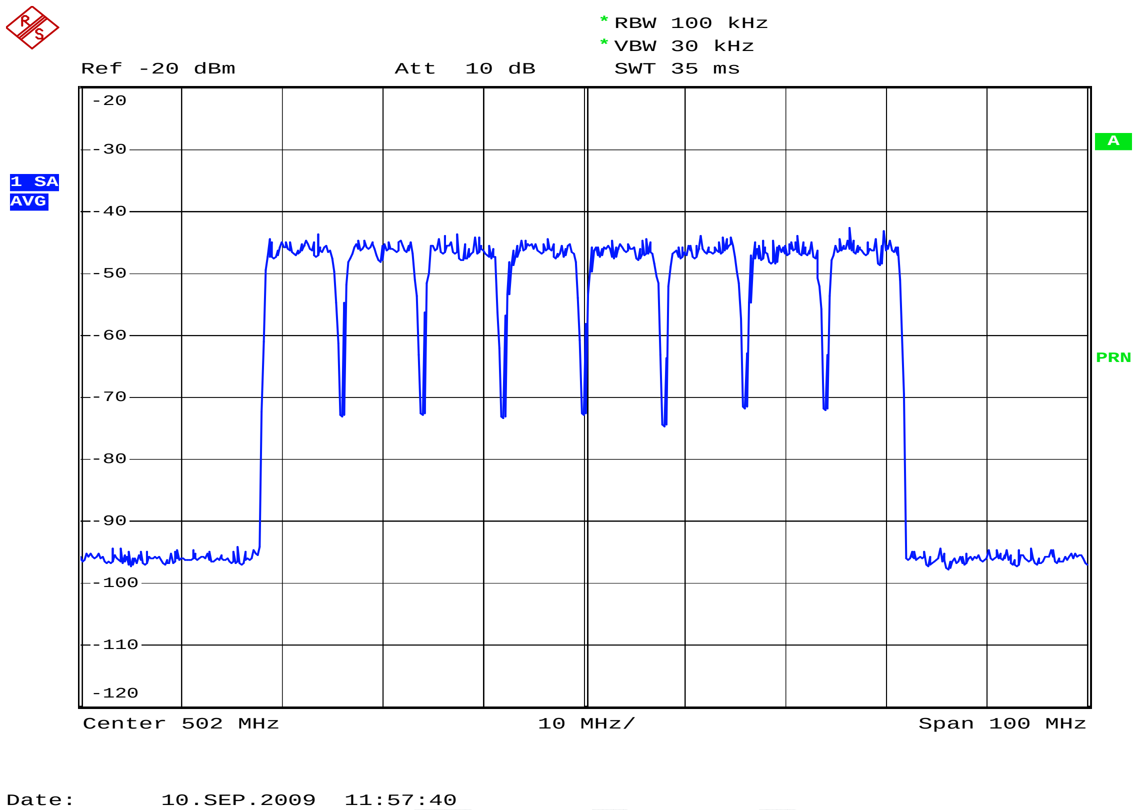
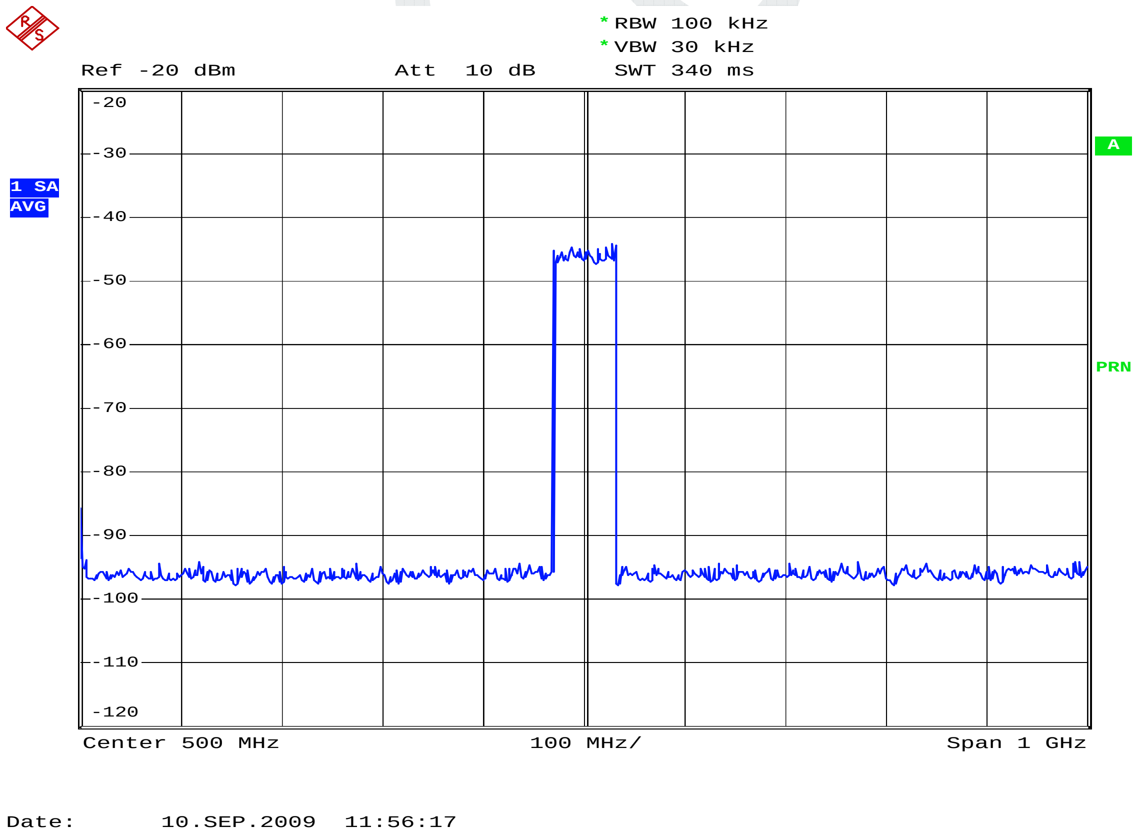


Screen 4a : 8 channel QAM, 6900MSps, 8MHz channel raster, 474MHz ff



Screen 4b : 8 channel QAM, 6900MSps, 8MHz channel raster, 474MHz ff, full band

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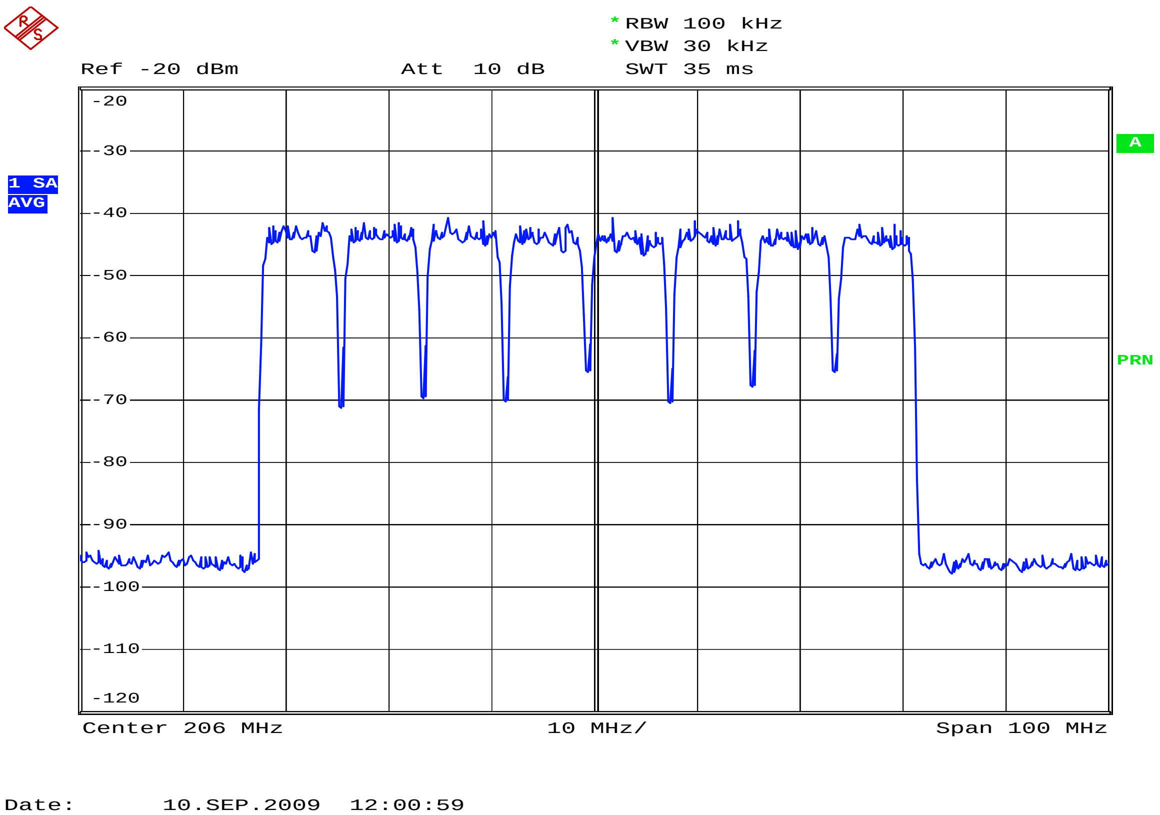
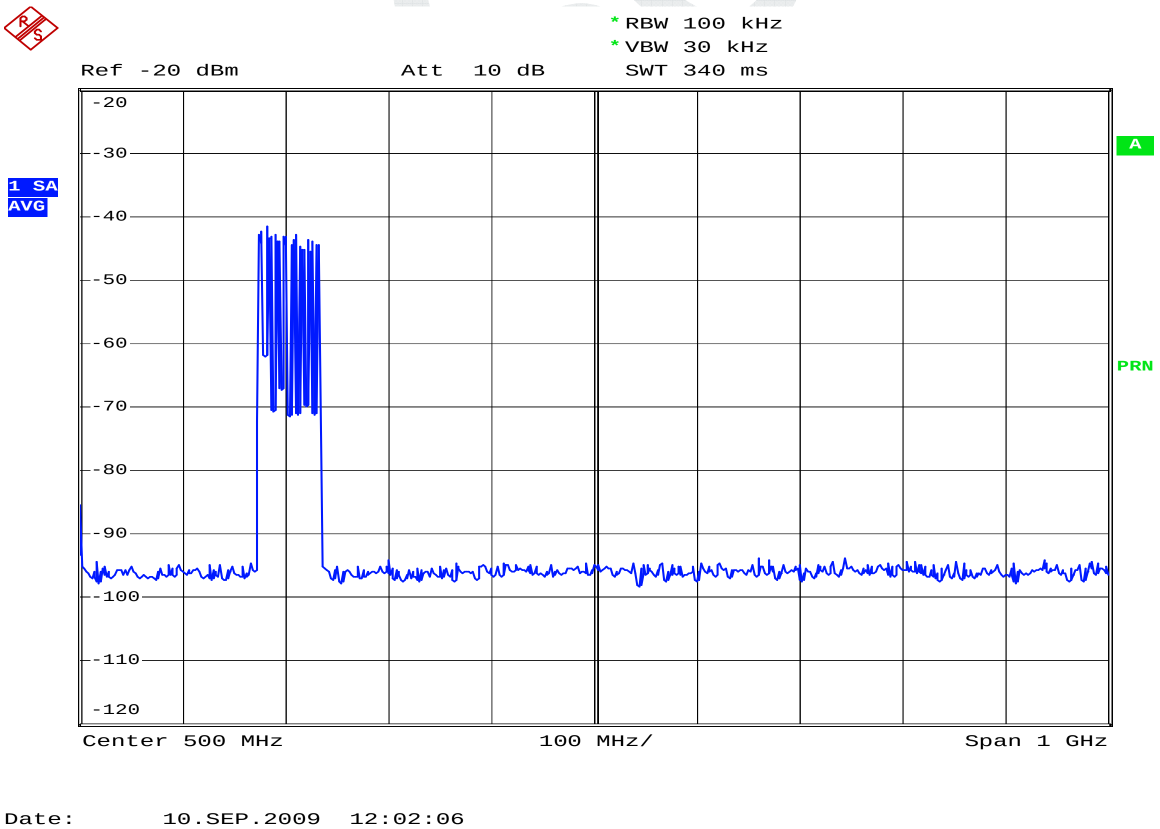


Screen 5a : 8 channel QAM, 6900MSps, 8MHz channel raster, 177.5MHz ff



Screen 5b : 8 channel QAM, 6900MSps, 8MHz channel raster, 177.5MHz ff, full band

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