

Adding access intelligence

Network processors are tackling growing challenges in the access network. By **Roy Rubenstein**.

Service providers continually upgrade their networks, but as soon as they tackle one problem, another arises. Given the rapid clip at which broadband traffic is growing, it is the access network that is demanding the operators' attention.

For wireless, uptake of 3G dongles and smart phones means operators are upgrading cellular sites to backhaul rapidly growing mobile broadband traffic. Meanwhile, the capacity of fixed broadband links to the home is also on the rise and broadband rates of 50 and 100Mbit/s are becoming common. Such traffic growth is leading to subtle changes in the access network.

While Ethernet is replacing the ATM and T1/E1 lines used for wireless backhaul, greater intelligence is needed to handle the various traffic flows. An operator's IPTV service is treated differently to a YouTube video delivered over the internet, but both streams have requirements different to voice packets. The access network must process the various packet payloads in a smarter way.

These developments explain why two chip companies – EZchip and Wintegra – are coming to market with network processing families.

EZchip's NPA family targets fixed access and wireless backhaul. "Until recently, our focus was the high speed segment – edge routers and switches further from the subscriber," said Amir Eyal, EZchip's vp of business development.

For fixed access, NPAs will process traffic from aggregation platforms, such as DSLAMs and fibre based passive optical networking units – or optical line terminals – that aggregate traffic from tens of homes or buildings. For wireless, the devices will process basestation traffic.

Meanwhile, Wintegra has launched the first members of two families: WinIP3, focused on fixed access; and WinPath3, for wireless applications such as LTE and WiMAX. These are Wintegra's third generation devices for access, tailored for Ethernet and IP. "By removing legacy support, we're removing cost from the WinIP3 devices," said Gordon Lawton, European sales and marketing director.

EZchip's NPAs are 10Gbit/s data plane processors that classify and route packets. They also have end to end network awareness – equivalent to supporting layers 2 to 4 of the OSI reference model.

The devices can buffer incoming packets, but

use external memory when scheduling outgoing packets. The NPAs are rated at 10Gbit/s, but can handle traffic over subscription: the NPA-3 has up to four 10Gbit/s ports and memory can be used to buffer packet bursts in excess of 10Gbit/s.

At the core of the NPA architecture are four 'flavours' of task optimised processors (TOPs): parsing; searching using look up tables; packet modification; and packet forwarding.

"These are smaller [than a risc core], so we can integrate more on a die," said Eyal. Each TOP has a 64bit architecture and processes a single thread. A scheduler allocates a packet to the next available TOP. While EZchip has not detailed the number of TOPs per ic, Eyal said the most numerous of the four is the search TOP. "For a given packet, there is a requirement to do lots of look ups."

Other on chip hardware blocks include a traffic manager and ternary content addressable memory (TCAM). As the name implies, the traffic manager makes decisions when packet congestion occurs, based on a given traffic's priority and rules it has been given. For example, a high definition video stream may have the highest priority regardless of other traffic, or the NPA device may be signalled by an edge router

Fig 1: NPA block diagram

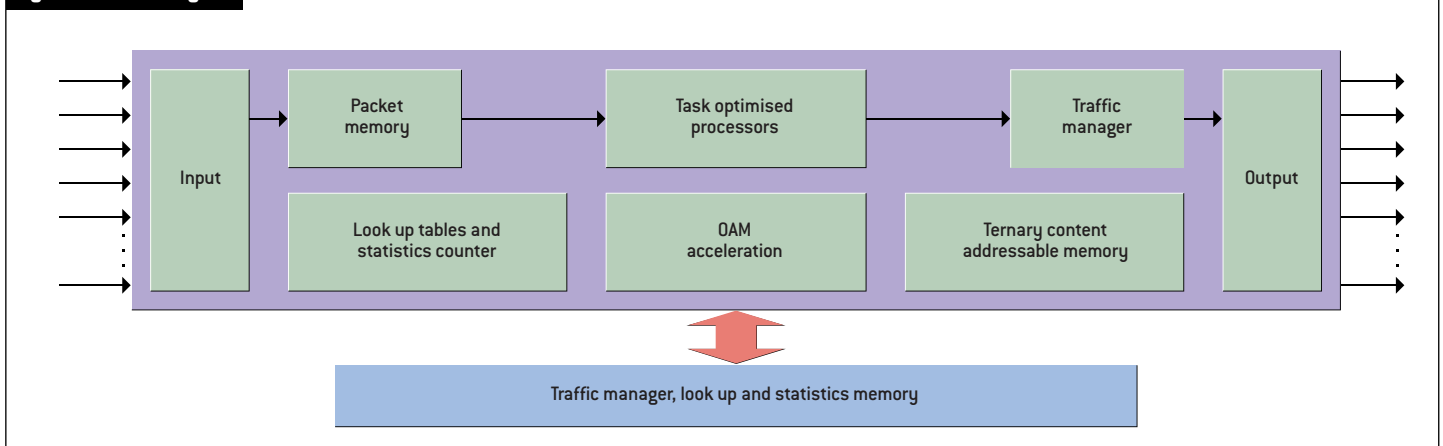
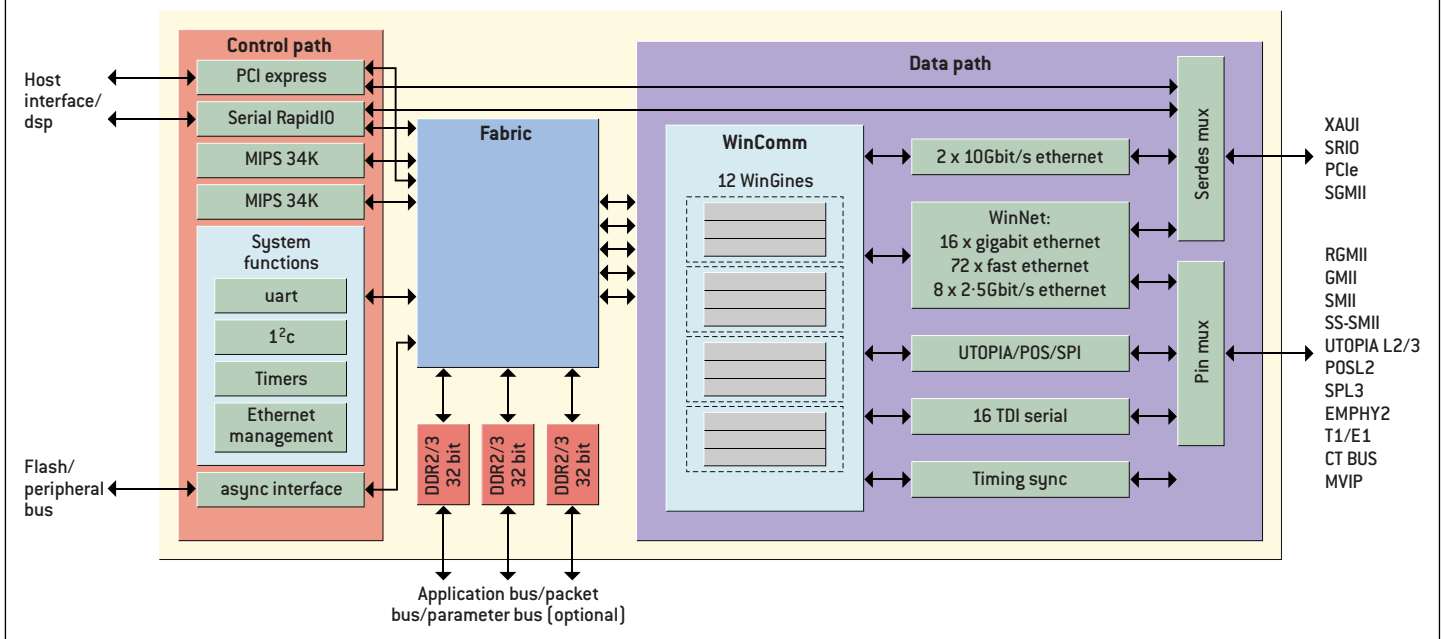


Fig 2: WinPath 3 block diagram



about traffic congestion and be told to throttle back packet traffic. The device will first store packets in its buffer memory before dropping lower priority packets once memory is full.

The on chip TCAM allows for sophisticated look ups to be performed and operates in parallel to the simpler TOPs based searches.

EZchip's three NPAs have various interface options to meet different designs. The NPA-1 supports eight 1Gbit/s Ethernet ports, the NPA-2 has 16 1Gbit/s Ethernet ports, while the NPA-3 offers several options: two 10Gbit/s and eight 1Gbit/s Ethernet ports; one 10Gbit/s and 12 1Gbit/s Ethernet ports; or even four 10Gbit/s Ethernet ports.

Wintegra's latest devices, meanwhile, extend the company's existing WinPath2, boosting processing performance by a factor of between three and five times. This is achieved by increasing the clock speed and added more packet processing engines – WinGines.

The new architecture uses 6, 9 or 12 WinGines clocked at 450MHz, and two 650MHz MIPS 34K processors. WinPath3 devices thus support control plane (layer 4 to 7) and data plane (layer 2 to 4) tasks and are rated at 10Gbit/s – 5Gbit/s duplex when processing 64bit packets.

"We have up to 12 engines that process as a uniprocessor," said Lawton. A hardware scheduler allocates tasks to the engines, called via an application programming interface running on

one of the MIPS. "Some 80 to 90% of our [code writing] customers don't go into the network processing engines," he said.

One of the MIPS risc cores can be dedicated to the data path communications – control and configuration, getting statistics and managing tables – says Lawton, while the second can handle the customer's application.

The WinGines are multithreaded, with each thread being an Ethernet packet. Tasks performed include receiving, classifying, modifying, shaping and transmitting a packet. "The engine is designed such that, on every clock, it is doing something useful," said Lawton.

The engines are programmed in a 'C' like language, such that the fundamental architecture can be used for wireline and wireless tasks. Wintegra devices do not include TCAM, instead they use standard DDR 2/3 memory. Some sram is integrated on chip.

WinIP3 has PCI Express, two 10Gbit/s Ethernet and up to 16 Gbit/s Ethernet interfaces, or 72 Fast Ethernet interfaces or eight 2.5Gbit/s ports. In contrast, WinPath3 also supports Serial RapidIO and legacy interfaces.

Both companies' families of merchant processors compete with fpgas and custom switch asic designs.

"There are alternatives, we are not coming to a greenfield market," said Eyal. "All are viable and all are being used." But he argues the NPU is the

most integrated and flexible when it comes to accommodating new features. "The customer is required to change the software versus redefining the fpga," he said.

Lawton also highlights the significant engineering effort of an fpga based design and agrees about an NPU's ease of modification. "There is always feature creep; dropping in a new protocol for 4G wireless into an fpga is non trivial."

EZchip says there will be more NPA members, targeting both ends of the processing performance spectrum. It is also possible that functions on the line card will be integrated. NPA devices integrate additional functions that would otherwise require a separate chip, for instance a fabric interface controller to connect to Ethernet switches used on the backplane in a chassis system. Additional functions on the line card could be integrated on chip, Eyal hinted.

Wintegra's roadmap will also expand both ends of the performance spectrum. At the lower end chip cost reduction could tackle smaller wireless cells such as femto and picocells, while higher end designs will be unveiled for next generation wireless and fixed access schemes, such as LTE and 10Gbit/s Ethernet PON.

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