

Keep in control

Accelerate time to market for system control applications with PLDs. By **Shantanu Dhavale**.

System designers are faced with continual pressure to meet their development schedules, and need to implement control functions with minimal effort and risk, while maintaining maximum flexibility. By using a programmable based approach for their designs, designers can accelerate their time to market, address system cost and space reduction and ensure a high level of product differentiation.

Designers need to minimise the total power dissipation of their system. Lower operating power means fewer board components, which reduces the total system cost. However, as process geometries migrate to smaller nodes, the power consumption of the device increases. This causes the total system power to increase, decreasing the mean time between failures (MTBF) of other devices on the board, thereby affecting the overall system reliability.

In response, designers are using sophisticated techniques to control power and temperature in their designs, such as dynamically adjusting the frequency, voltage and airflow dependent on the system load and operating conditions.

In addition to actively managing power, frequency and airflow, there are a number of benefits to monitoring and logging environmental conditions such as temperature and voltage. Changes in these variables can be an early warning of likely failures. After failure, this information can be useful in debug and repair. Many manufacturers also use this data to determine if a warranty placement is justified or not.

Boundary scan, defined by IEEE1149.1, is a standard method for testing interconnects, monitoring pin states, or testing the logic status of components on a pcb. It is a probeless technique that allows testing of hardware via Jtag commands.

Designers typically test Jtag chains one board at a time. However, with multiple boards to support

high levels of functionality, testing long chains presents challenges. A failure on one chain can cause the entire system to become non testable, as fault detection and isolation can be quite difficult. Also, physical routing while trying to balance skew and voltage translations between different devices can be difficult.

Updating logic while devices are deployed in the field continues to be important as it provides designers the flexibility to respond to changing standards, fix bugs, upgrade existing equipment and minimise system downtime. Systems are typically placed in a non operational mode while the logic is being updated. However, system manufacturers are under increasing pressure to increase system up time. In fact, in many system control applications, the demand for 'five nines' (99.999%) up time is common.

Many designers are using plds to implement system control functions. Typical pld requirements for these applications include:

- Low cost
- Simple single chip solution with on chip flash

- Operation often possible from a single 3.3V power supply
- Distributed and block memory
- PLLs
- Flexible I/O supports common lvcmos interface standards

The following sections discuss how plds can be used to address the trends outlined in the previous section. Although each is presented independently it is important to note that in many cases, designers implement multiple solutions inside a pld.

PLDs are ideal for feedback control operations due to their:

- Ability to power up that enables precise control during system boot-up
- High I/O count for monitoring and controlling many signals to multiple devices

Some plds can make it simple to implement these types of functions. For example, to implement temperature based fan control, Lattice's MachXO PLD, in conjunction with



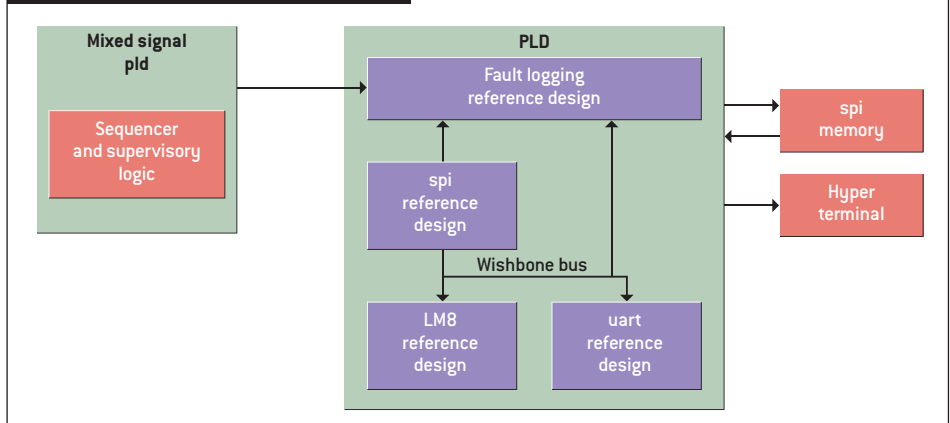
i2c temperature and PWM controller reference designs and a mosfet, can control the speed of the fan, enabling temperature regulation within a system without the need for an external sensor.

PLDs, used with mixed signal plds and spi flash memory devices, provide a solution for logging environmental variables such as temperature and voltage. Systems can be designed to continuously log data or to log data only when predefined limits have been exceeded. Figure 1 shows a block diagram of the fault logging design using plds. In this example, the fault log can be interrogated via the serial port.

Designers typically use discrete a/d converters to monitor the various sensors and power rails of a system. Delta Sigma a/d conversion is an efficient and cost effective way of replacing discrete devices and of monitoring voltage fluctuations on a board. The design can be implemented using a pld. Designers can modify parameter values to define the bit precision and adjust the sampling rate of the a/d converter. Figure 2 shows how a pld can be used to implement voltage monitoring using Delta Sigma a/d converter.

Some plds support this capability through the use of flash and sram technologies on a single chip. Using the flash memory, some plds can be programmed in the background while the device continues to operate. The device's sram controls device configuration, while the flash is updated in the background mode. The I/O states are usually maintained during device programming to allow seamless transitions while updating the logic from sram to flash. The new configuration file can be

Fig 1: Using PLDs to log environmental data



loaded into the sram logic, enabling remote field upgrades and minimising system downtime. Using Lattice's MachXO plds, for example, the sleep pin (SLEEPN) can also be toggled to load a new configuration file into the sram logic without having to cycle the power. The sleep pin is also useful in power sensitive applications and controls the power down or sleep mode of the device. Using the sleep pin, the static power of the MachXO pld is less than 100µA.

Development kits and reference designs provide a comprehensive platform for prototyping with plds in system control designs. Some pld vendors provide preloaded designs that demonstrate board control functions. For example, Lattice's MachXO Control Development provides a preloaded control system on chip [Control SoC] design implemented in the MachXO PLD and includes board control functions such as fan

speed control based on temperature monitoring, lcd control, power supply monitoring and reset distribution in conjunction with the Power Manager II POWR1014A and 8bit LatticeMico8 microcontroller

Using the Control SoC design, designers can test board control functions within minutes and then build their own designs using the free downloadable reference design source codes, implementing these features in less than an hour.

Reference designs optimised for control and interface bridging functions can be downloaded for free from a pld vendor's website. Most of these reference designs include support for popular protocol and connectivity standards such as i2c, spi, uart, PCI, power fault logger and Delta Sigma a/d converter. The reference design source – including HDL, firmware and design tools – can be modified, depending on the application requirement.

PLDs are ideal for implementing system control functions such as temperature measurement, current monitoring, power supply sequencing, fan control and maintaining environmental data logging, commonly found in communication, wireless infrastructure, high end computing, industrial and medical applications. They provide several key system integration benefits that ultimately reduce total system cost. Development kits and reference designs provide designers a comprehensive and flexible solution to accelerate their system control designs quickly and effectively.

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Fig 2: Voltage monitoring using a PLD and a Delta Sigma a/d converter

