

# Another dimension

How programmable logic is adding another dimension to its abilities. By **Graham Pitcher**.

**W**ith the ability to be designed relatively easily and then to be reprogrammed as required, you might have expected programmable logic to have become a more dominant technology than it is today.

There's a number of reasons why this hasn't happened, but the main reason is generally agreed to be cost; while the ability to reprogram devices is attractive, this cost is not attractive in volume applications.

FPGAs are relatively large and more silicon means more expense. So, while they offer the benefits of reprogrammability, they can't compete with ASICs when it comes to volume pricing. Many companies would like to use FPGAs in volume, but simply can't afford them.

So one of the challenges for programmable logic over the years has been for the technology to reinvent itself in a format where its benefits are available at competitive cost. A number of companies have picked up the gauntlet, but have failed and the market remains one dominated by Altera and Xilinx, with a share of around 80% between them, and a collection of other companies chasing the remaining 20%.

But two new entrants into the programmable logic market believe they can change things and both companies – Tabula and Tier Logic – believe they can do this using a third dimension. The difference between the two is their definition of that third dimension: Tabula defines it as time, while Tier Logic defines it as physical depth.

Alain Bismuth, vp of marketing with Tabula, believes one of the major challenges has been software. "Most of the companies which have failed have underestimated the challenge of developing software that works and which doesn't change the way users design FPGAs."

Paul Hollingworth, vp of marketing for Tier Logic, had a similar story. "Our Mobius tools have the same features as those from existing FPGA providers and the design flow is exactly the same. New or existing designs [can be] synthesised, packed, placed and routed into Tier Logic devices using industry standard design tools, such as Precision Synthesis from Mentor Graphics."

The phrase 'place and route' is crucial. Bismuth remarked: "Tabula founder Steve Teig realised the 3d problem could be solved by treating it as a classic timing driven place and route problem."

So what is involved in going 3d? As mentioned, Tabula says it's all about time. "Time is the third dimension," Bismuth asserted. "3d is interesting because the major contributor to cost is area. The smaller the area, the lower the cost and the better yield. Tabula emulates the third dimension by reconfiguring the device up to eight times per cycle. In this way, the chip is reused as much as possible."

Claiming the whole device can be reprogrammed in less than 80ps, Bismuth said the Spacetime architecture allows space to be traded against time, density and performance.

"Our software will look at the RTL and determine which portion is performed during each eighth and will generate configuration code automatically that allows the device to perform the given tasks."

The basis of Tabula's approach is 'folds' (see figure 1). Each fold performs a portion of the desired function and stores the result in place. When some or all of a fold is reconfigured, it uses locally stored data to perform the next portion of the function. By reconfiguring the part to execute different portions of each function, a Tabula FPGA is said to implement a complex design using only a

**Fig 1: How Spacetime creates a third dimension**

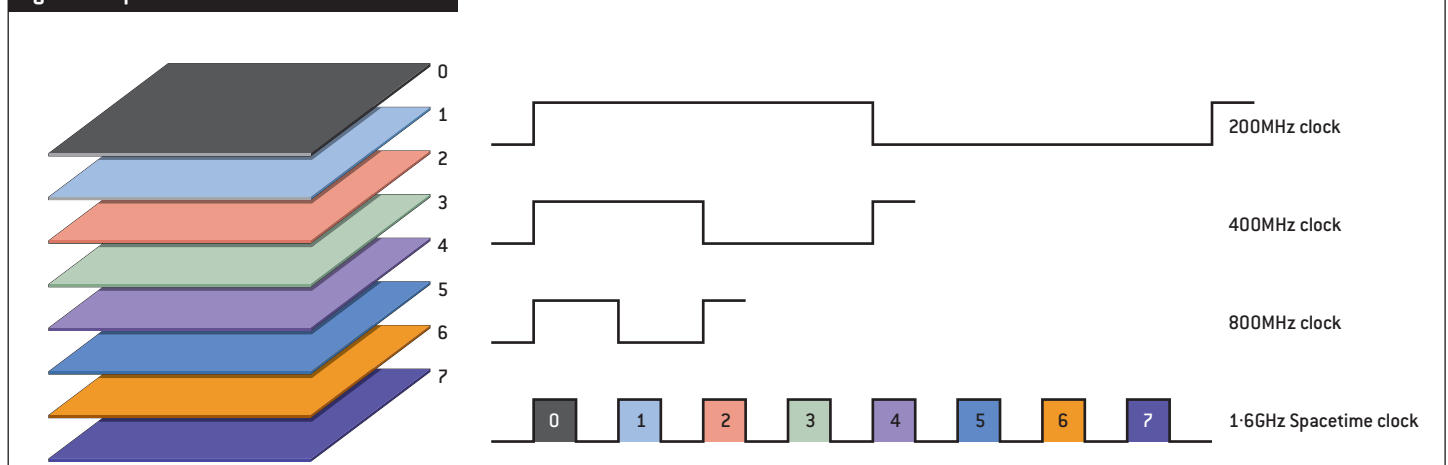
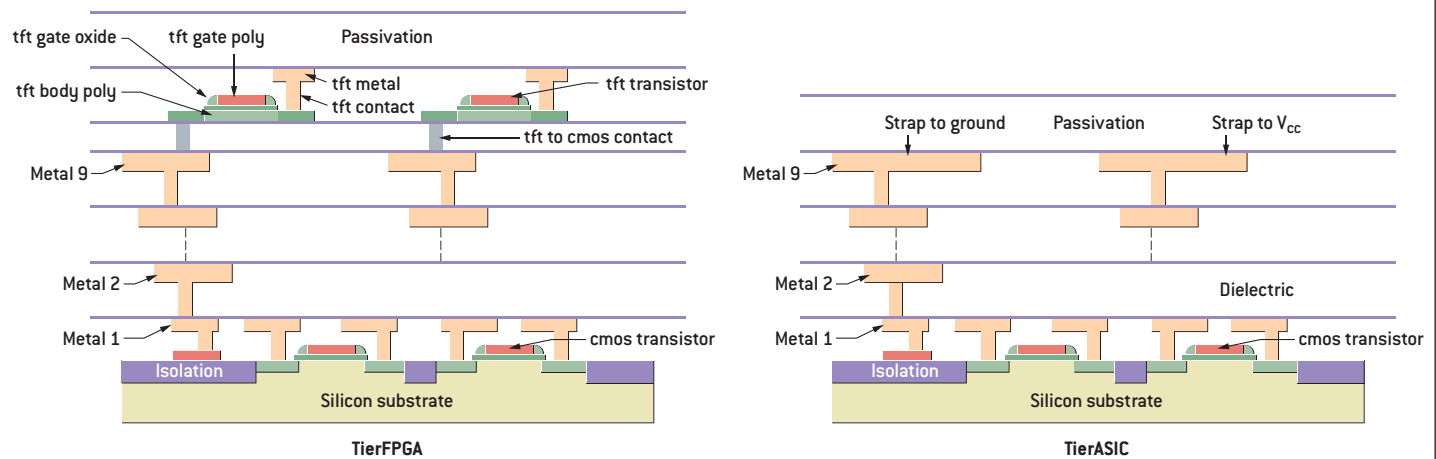


Fig 2: Tier Logics's fpga and asic solutions



small fraction of the resources that would be required by an inherently 2d fpga.

Bismuth explained: "If you have task A on fold 0 and it tries to connect to task B on fold 3, you know the delay between the LUTs and the time taken to reconfigure three times. It's basically a via in time."

Tier Logic, by contrast, is building upwards. Hollingworth noted: "An fpga is planar, with user logic and configuration logic. Configuration logic takes up more than 50% of the transistors in a modern fpga. If we can put those on another layer using thin film transistor technology, we can shrink die size."

Tier claims that its technology allows users to either take advantage of a larger device for the same cost or to take a design into a smaller device. For the moment, the company is using a 90nm process to minimise risk, but Hollingworth said the technology 'scales better than cmos'. "We could go to 40nm," he added, "but it's a balance between how small should the tfts be compared with the area in the base array." Nonetheless, Hollingworth believes TierFPGAs bring an x3.5 performance advantage over current fpga implementations.

Tabula, by contrast, is at the 'bleeding edge' with its ABAX products being fabbed on a 40nm process at TSMC. It needs this process to support the potential maximum clock rate of 1.6GHz. And Bismuth believes pushing down to the next node will be a rewarding move. "Suppose we went to 28nm," he conjectured. "We'd be able to support 2.4GHz, which brings 50% more performance, and could turn eight folds into 12. That could bring an

x3.7 advantage. At 22nm, that could be an x5.5 advantage."

It is this move to the third dimension – whether time or height – that both companies say makes their technology a suitable candidate for changing the dynamic of the fpga market.

Both are keen to point out the shortcomings of traditional fpga technology, as well as those of the asic. Hollingworth again: "We used to talk about the design phase and the production phase.



FPGAs were ideal for the design phase, but not for production and vice versa for asics."

Bismuth added: "ASICs and fpgas are equally unsatisfactory. ASICs are good for low unit cost, but take time to develop and, when you're done, it's fixed function. FPGAs are flexible, with short times to market, but are too expensive for production."

But that's the extend of their agreement. Where Tier Logic offers TierFPGAs and TierASICs, Tabula offers the one device.

Tier Logic makes changes at the top of the stack to create an asic. "Once the design is stable,"

Hollingworth explained, "the programmable configuration circuitry layer can be replaced by a simple metal layer and the design turned into an asic. However, because the timing remains identical between the fpga and asic, it allows zero risk, zero effort conversions. That's unlike structured asics, where timing is different from the original fpga."

Bismuth claimed Tabula's ABAX range can cater for both applications. "It allows programmable logic to be used from beginning to end, with a price that is near enough to allow it to be used in full volume, but to be used just like an fpga."

Addressing the cost issues, Hollingworth claimed a design implemented in a TierFPGA can be up to 50% cheaper than when implemented in a regular fpga. "And a TierASIC will then be another 50% cheaper, with an NRE of only \$25,000."

Bismuth said ABAX devices offer 'two to three times the performance of fpgas at less cost'.

According to Bismuth, Tabula already has a design win with a Tier 1 OEM in the communications market, with products set to be released later in 2010. Hollingworth pointed to three TierASIC designs being fabbed. "One of these includes a MIPS R4000 core," he claimed, "the other has a SPARC subsystem."

But will Tier Logic and Tabula succeed where many other have fallen by the wayside? Time – appropriately in Tabula's case – will tell.

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