

Delamination is a potential problem in 3d packaged chips

Packing potential

Package choice is a critical aspect of the semiconductor design process. By **Graham Pitcher**.

The delicate pieces of silicon which enable the functionality we take for granted have to be encapsulated in some way or another and the signals they process routed to and from the host pcb. Because package performance can be a limiting design factor, selection of the best package for the job starts at the same time – or even earlier – as silicon design.

Knowing which package is going to be used helps the designer to take such factors as parasitics and thermal effects into account. But other factors are becoming increasingly important as consumer electronics devices get ever smaller – and profile is one of the critical dimensions.

Mark Jacob is director of marketing for Dialog Semiconductor, which focuses on power management and other mixed signal devices. “Packaging is key, particularly in relation to thermal performance,” he noted, “but the three main considerations when selecting a package are cost, performance and form factor.”

Sandeep Kumar, vp of operations and engineering for Silicon Labs, told much

the same story. “At a high level, our strategy is to come up with disruptive products. To do that, the number one thing is design creativity and the choice of process and package, along with cost and performance, is critical.”

Jacob said meeting design goals means Dialog has to work closely with packaging houses and subcontractors. “We look at a range of packages to support new products,” he pointed out, “and one of the key drivers at the moment is high I/O density. As you integrate more functions, the number of pins increases.”

KUMAR: “DIE SIZE AND PACKAGE SIZE ARE CRUCIAL [IN CONSUMER ELECTRONICS].”

Kumar said that, in some cases, the designers already know what package will be appropriate. “We then start working backwards in order to determine die size. In other instances, we match what the customer wants. Either way, packaging is a key part of our decision making process.”

Jacob pointed to the DA9057, a recently introduced power management ic. “This has a peak current handling capability of up to 5A. At that level, we can’t internalise individual regulator supplies, which means a higher I/O count is needed.”

Because Dialog is looking to maximise performance, parasitics are a consideration. “Where you have a current path of many Amps,” Jacob continued, “a few Ohms of contact resistance is significant, leading to voltage drop and lower efficiency.”

Kumar claimed that, given the choice, SiLabs would select a mature packaging technology. “But it doesn’t work out like

A dual row qfn package satisfied engineering and marketing requirements for this power management ic



that," he pointed out. "Sometimes, we have to go for a special design."

One critical market for all companies is consumer electronics. Kumar noted: "Die size and package size are crucial here, especially for mobile phones and tv. It's part of our decision making process that if we can't make it small enough, we won't make it."

Currently, SiLabs is developing chips for ultra thin tvs. "That market is driving very small packages and SiLabs is coming up with devices in quad flat no lead (qfn) packages, while competitors are still using cans."

For SiLabs' timing products, however, it's all about size and cost. "Because there's a crystal," said John Pavelka, principal packaging engineer, "we need hermetic packaging, but there aren't many thermal and signal integrity issues. Neither do these products run at frequencies where they need special impedance control. Because of this, we're using qfns."

It's much the same story for microcontrollers, said Martin Gabriel, senior packaging engineer. "There aren't really any thermal issues, so package and cost are drivers. The main difference is that, with a range of customers, every die must be available in a choice of small pitch, small packages, as well as in leaded types."

Jacob noted that it's not just the package. "Customers also look at the system, including external components, to determine the pcb area. So we may need to use a smaller package with a smaller pitch in order to compete."

Selecting the right package is a balancing act. Jacob gave an example. "In the DA9052, a dual row qfn, with a thermal slug soldered to the pcb, provides an improvement of about 8 to 10K/W in thermal performance, compared to the same footprint bga. This means higher currents can be handled for the same temperature range. That satisfied engineering requirements.

"Because the package also met customers' footprint and unit cost goals, that satisfied marketing requirements."

Stressful moments encountered during 3d packaging development

Pol Marchal, principal scientist in imec's 3d SoC design initiative, says packaging developments are being driven by applications.

With new data services – such as video transfer – driving a rapid increase in demand for bandwidth, Marchal believes devices will need to support data transfer rates of 12.8Gbit/s in the near future.

But mobile phone developers want packages in their products to be less than 0.6mm high. To meet these demands, Marchal said: "We are looking at creating a stack with two dram dies mounted on logic, with everything on a flip chip bga substrate."

He believes a device can be created which not only meets bandwidth and profile requirements, but which also consumes less than 0.5W. "We have demonstrated a 3d network on a chip and the technology is now at the point where we can start building working circuits." He envisages the drams being only 30 to 40µm thick, with a microbump pitch of 10 to 20µm. Through silicon vias (TSV) will be only 3 to 5µm wide [see fig 1].

However, one problem to be solved is the stress created during the manufacturing process, which can result in delamination. Marchal noted: "We need to design for this and determine how to control it."

Even though the copper TSVs needed to link the various dice are less than 5µm wide, they have a different coefficient of expansion to the wafer and this can affect device performance at the transistor level. "We will need to keep devices away from TSVs in order for them to work properly," he concluded.

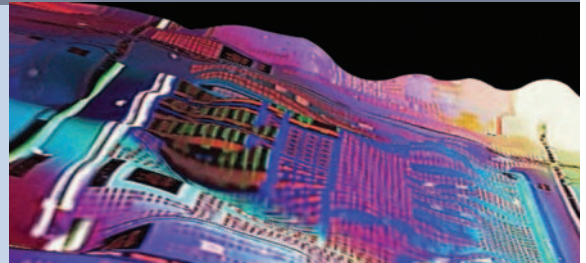
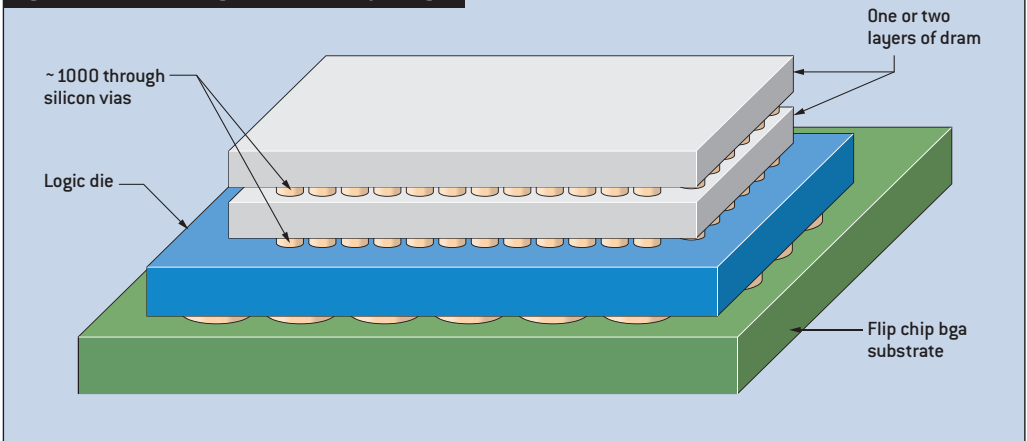


Fig 1: How imec envisages multidie TSV packages



When real estate is at a premium, companies may need to build upwards, while bearing in mind the need for thin packages. "We are moving more and more towards systems solutions," said Kumar, "taking an mcu, combining with a high voltage chip, short range wireless and Power over Ethernet and building multichip modules. But we're putting them into qfns and it's a relatively mature process. We're working with best in class packaging houses and we

JACOB: "THE THREE MAIN CONSIDERATIONS ... ARE COST, PERFORMANCE AND FORM FACTOR."

minimise risk by going with those who give the flexibility and price we need."

Jacob accepted that stacking dice brings another option if earlier trade offs don't work. "It depends on the application, but there is a lot of momentum behind system in package. It allows a higher level of integration in the short term."

"Packaging," Jacob concluded, "is driven from different directions and it's quite an interesting balance. It's all about finding the right trade offs."