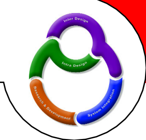


Dielectric difficulties

High K solution needed this year if cmos is to hit 45nm on time. By **Paul Dempsey**.

Sometime this year, the talking will have to stop. Somewhere in the industry, a company will 'process lock' on an approach to the manufacture of a high K dielectric/metal gate stack. Either that, or the semiconductor industry will have to admit to something of a defeat.

If anyone can make the leap, it's likely to be one of the leading players – Intel has been very aggressive on its plans to introduce these stacks. Because, despite some initial controversy, the high K/metal recipe is now seen as critical for the 45nm node, which those big suppliers would like to hit by 2008.

The flurry of associated research is also an example of the latest phase in the battle between Moore's Law and the longer entrenched Laws of Physics. The reality is that, right now, the 'Stop' sign is looming.

Firstly, let's recap the fundamental high K issues, even though the topic is more than a decade old.

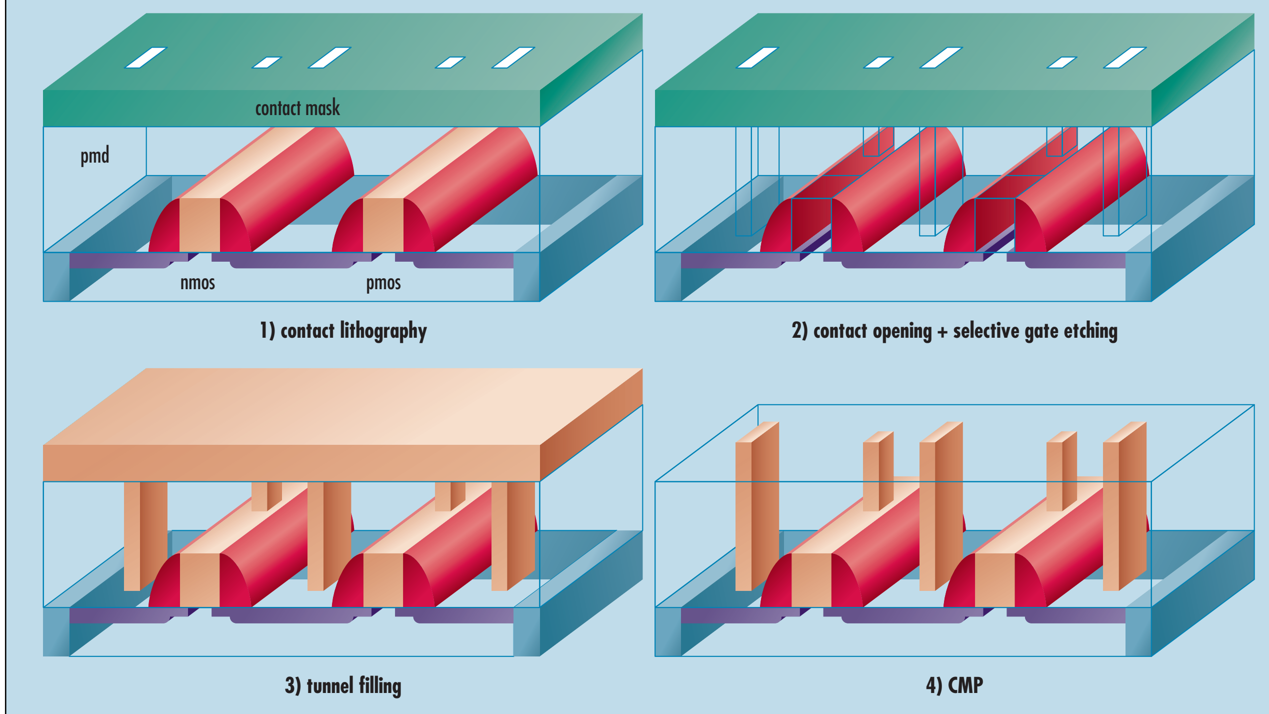
The 90nm node has taken the thickness of the SiO_2 dielectric layer to 1.2nm. At 45nm, that will be closer to 0.8nm. As thickness approaches SiO_2's molecular level, quantum tunnelling current leakage comes into play. Unacceptable levels of power dissipation and heat generation are the two most significant results.

What chip manufacturers want, therefore, are usable materials with a K (or dielectric constant) greater than the 3.9 of SiO_2 (hence 'high'). Such a material must offer greater capacitance and a sufficient molecular/atomic thickness to prevent – or at least mitigate – tunnelling. Several candidates have emerged, including hafnium oxide, titanium oxide and zirconium oxide.

The problem is that such materials tend not to marry too well with traditional polycrystalline silicon (poly Si) electrodes. The biggest issue is Fermi level pinning. Here, gate depletion defects, that emerge at the meeting point of the dielectric and the transistor, push up the threshold voltage and damage performance.

A second less serious, but still important, factor is phonon scattering. Higher K values mean higher polarisation; that, in turn, creates surface optical phonon

Figure 1: The PRETCH process



vibration, which degrades electron mobility. So, performance takes another knock.

The proposal has therefore emerged to remove poly Si and replace it with a metal gate – silicided nickel being widely favoured. Interface defects are avoided and such materials can also greatly reduce phonon interference. Easy to describe – not so easy to do cost effectively for semiconductor production.

And there is a further twist: 'n' and 'p' transistors require different metals tuned to different work functions. Doping proposed metal gates so this range matches poly Si is also proving a challenge.

As Intel fellow Robert Chau has observed, what his company and others are attempting to achieve is 'a heart transplant for the semiconductor industry'.

At the 2004 International Electron Devices Meeting, held last December in San Francisco, two aspects of the state of the high K art were evident.

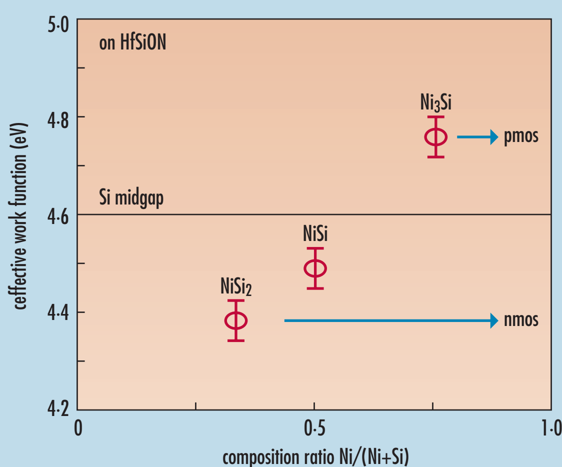


Figure 3: Nickel silicide electrode work functions

Nobody has yet 'locked' this part of the production process, although everyone accepted that, for 45nm, fab equipment suppliers would need to hear something before the end of 2005 in order to get a three year start on the roadmap.

However, the more positive news emerged in work presented by NEC and STMicroelectronics, both of which presented high K/metal gate stack research broadly compatible with existing cmos manufacturing.

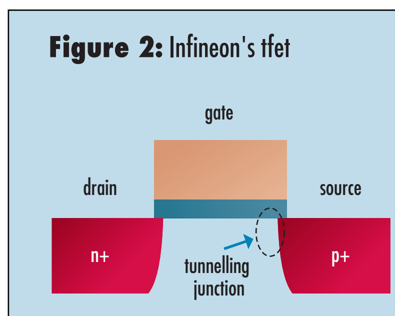


Figure 2: Infineon's tfet

NEC first fabricated pmos and nmos transistors, then applied varying thicknesses of nickel film by sputtering. Ni silicide gates were then formed by annealing. However, it was the earlier step that delivered the most interesting results.

Work function tuning

"By simply changing the thickness ratio of Ni to poly Si, several types of Ni silicide with different phases were formed," said Yasunori Mochizuki, senior manager of NEC's system devices research laboratory.

Introducing the dielectric and then analysing the resulting chip in more detail, NEC not only found a work function tuning range for the Ni silicide electrodes on the hafnium silicates, but also that the dreaded Fermi pinning based voltage shift was dependent on the silicide's composition. And this, NEC now knew, it could control to some considerable degree.

"Excellent transistor characteristics – such as sub threshold current, carrier mobilities, and low gate leakage – have been achieved. In addition, the performance of the gate stack structure ensures its feasibility of up to 45nm node low standby power and low operation transistors," Mochizuki said.

However, a question remains as to how close the Japanese company is to putting its lab work on a manufacturing line. In its official statement, NEC notes it 'will continue to make advancements in this research towards the realisation of *future mass production* of these new transistors' (our italics).

PRETCH, (Poly gate Replacement Through Contact Hole), the high K metal process flow unveiled by STMicroelectronics – from work undertaken with Philips Semiconductors, L2MP and CEA-LETI – adheres even more closely to the principles of cmos manufacturing. Indeed, ST's Philippe Coronel described the team's 90nm experiments with the technology as 'classical', with the exception of one step – the poly Si's removal.

"We start with a conventional flow gate etch," he continued, "but then open the contacts [over the chosen poly Si devices] with lithography and etch out the poly Si with an SF_6 plasma. This creates a buried cavity to fill with any gate material."

PRETCH has been validated so the poly Si and any initial gate oxide can be stripped and replaced with the metal gate and high K (or other) dielectric. Similarly, various materials or thicknesses of material can be integrated within the same process – an early objective was one architecture capable of holding three different gate stacks.

Another paper with input from ST and Philips also showed progress on the tuning range challenge, by approaching it from the total silicidation of a doped poly Si gate with nickel.

However, the impression remains the subject is still at the 'bitty' stage. Indeed, there remained enough space in the debate, despite the supposedly looming deadline, for Infineon Technologies to have used IEDM to put forward a full high K workaround – at least until 20nm.

It has proposed a tunneling field effect transistor (tfet), based on the principles of quantum mechanics. The architecture features a tunnel junction at the source side of the channel (see figure 2). In the non conducting tfet, a large pn diode barrier exists between source and drain, leading, Infineon says, to very low leakage currents. When a channel is formed by forward biasing the gate, a Zener tunnel current evolves with a steep turn on characteristic.

An effect typically seen as parasitic in other architectures – and akin to the obstacles facing a traditional SiO_2 dielectric – is here turned to a device's advantage. Moreover, the tfets were made using a standard and unmodified silicon process.

Printing teeshirts that ask: "Have you locked on high K yet?" is probably out of the question.