



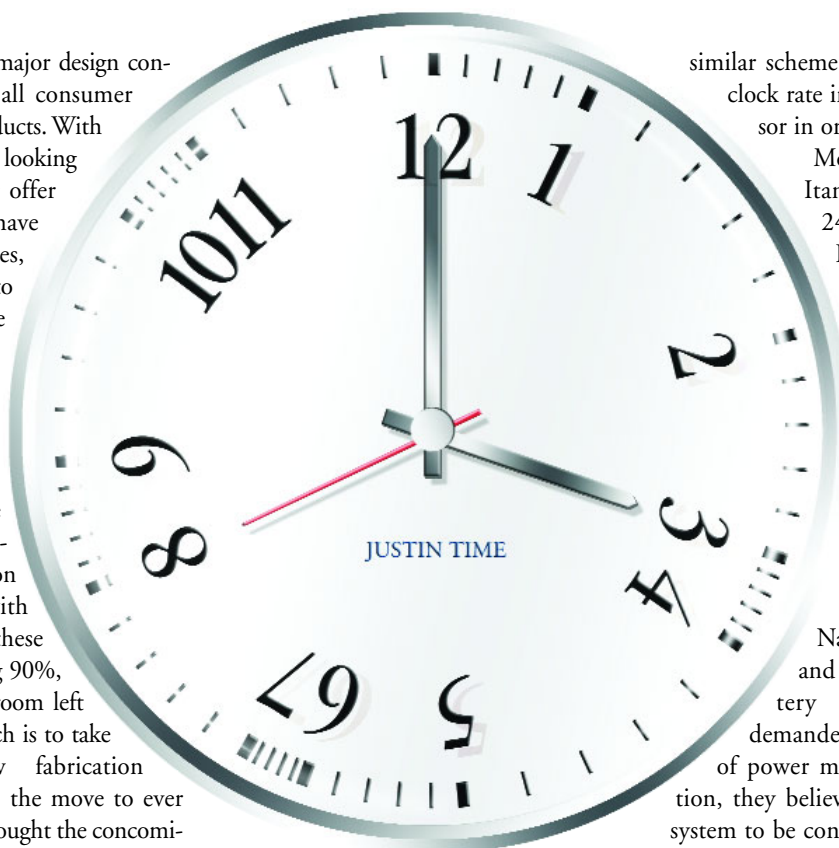
Time to **save** power

Battery life is a major design consideration for all consumer electronics products. With consumers, in general, looking to buy products that offer more features, yet have longer operating lives, designers are having to be more creative in the way they squeeze as much from the battery as possible.

One possible approach to the problem is to use ever more efficient power conversion and regulation components. But with the efficiencies in these devices now exceeding 90%, there is not a lot of room left here. Another approach is to take advantage of new fabrication processes. In general, the move to ever smaller features has brought the concomitant benefit of lower power consumption. But as components move to the 90nm node, physical effects such as leakage have somewhat negated these benefits.

What other approaches are possible, then? A promising avenue of research is asynchronous logic, where the performance of individual blocks of logic is decoupled from a global clock. Logic obviously consumes energy when it is switching on and off. If you turn the logic off when it isn't needed, you save power. Academics like Professor Steve Furber of Manchester University, and companies such as the Philips' spin out Handshake Solutions are making progress here (see NE, 23 Nov 2004, p45).

But a halfway house exists, where continuous adjustments are made to a



Adaptive control of frequency and core voltage is aimed at saving battery life in portable products.

By **Graham Pitcher.**

processor's supply voltage and clock speed in order to optimise power consumption. PowerWise, a joint development unveiled in 2003 by National Semiconductor and ARM, is one instance of this approach. But at this week's International Solid State Circuits Conference (ISSCC) in San Francisco, Intel is presenting further details of a

similar scheme in which it varies the clock rate in its Montecito processor in order to save power.

Montecito features twin Itanium cores and 24Mbytes of L3 cache; Itanium is the 64bit processor developed by Intel and Hewlett-Packard with the server market in mind. In all, a Montecito processor features 1.7billion transistors.

Radical rethink

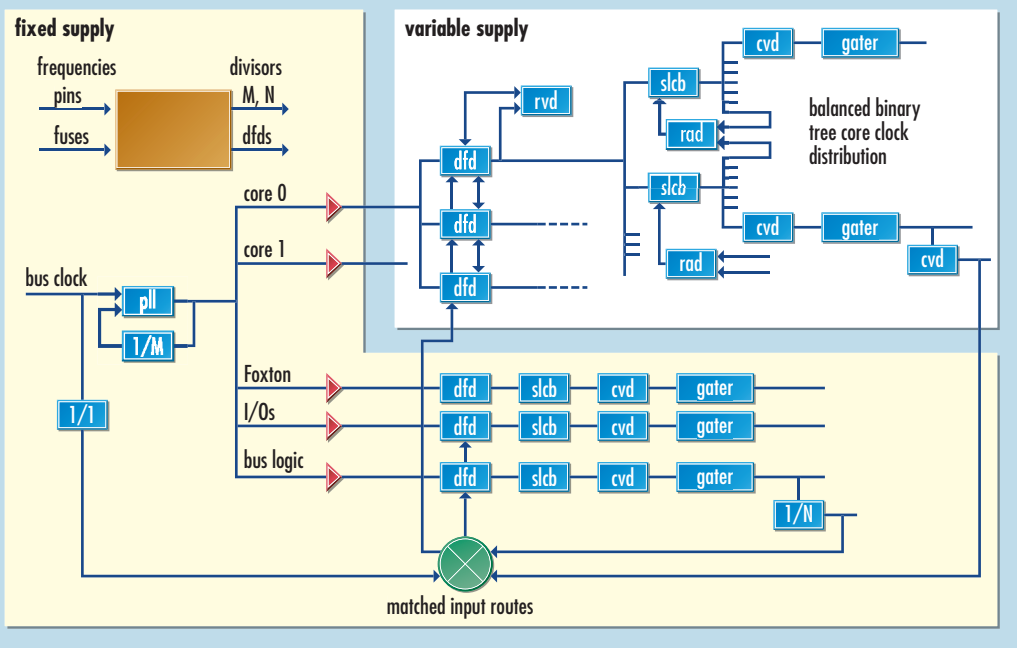
In the view of National Semiconductor and ARM, solving the battery lifetime dilemma demanded a 'radical rethinking' of power management. The solution, they believed, was for the entire system to be considered as a whole and for system components to work together to produce the desired power/performance level.

PowerWise is that system level approach. It aims to reduce the power consumption of a chip by creating closed loop systems in which power consuming digital ics and power delivery systems operate together to achieve peak energy efficiency.

Juha Pennanen, a system architect with National Semiconductor, has been closely involved with the development of the PowerWise concept. He said target applications for the technology would be battery operated devices with significant amounts of digital processing. "Mobile 'phones are a prime example," he said, "but you can also think of media players, digital cameras and hand held games."



Figure 1: The Montecito clock system topology



Where PowerWise differs from Intel's proposed system is that it is delivered as IP; Intel's variable frequency clocking system is designed as part of the chip.

Pennanen continued: "PowerWise is an adaptive closed loop voltage scaling technology targeted at systems that can change the processor's clock frequency and where there is the possibility of voltage scaling."

According to Pennanen, an older approach to the problem used look up tables. "But that's a static approach," he noted. "With PowerWise, voltage can be determined in real time and, because of that, it can take advantage of the properties of the die in its operating environment."

And, because PowerWise is IP, it can be used on any synchronous digital logic device, which extends its use beyond systems on chip and microprocessors into the dsp world.

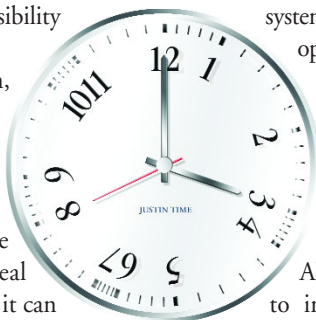
PowerWise technology embeds a synthesisable AMBA compliant core – the Advanced Power Controller (APC) – on the digital chip. The APC monitors and adjusts the chip's supply voltage so the

supply voltage is always optimised for the current operating frequency.

The APC interfaces to the rest of the system using two standard interfaces: the AMBA compliant host interface; and the open standard PowerWise Interface (PWI). The host interface passes performance requests to the APC from the host system and coordinates the APC's operation with the clock management system. The PWI interface communicates power management information to external power management devices to adjust supply voltages. The APC then enables the system to implement either dynamic voltage scaling or fully adaptive voltage scaling on the target system.

Standard interfaces enable the APC to be embedded into any logic circuit and interfaced with other parts of the system.

Robert Fischer is National Semiconductor's product marketing manager for portable power systems. He noted that PowerWise needed an 'ecosystem' in order to grow. "We needed partners in simulation, we needed partners in verification. We've made those partnerships."



In fact, there are six companies involved in the PowerWise initiative, including National and ARM. However, Pennanen would not name the others.

Foxton brings a boost

Intel's Montecito chip also features its Foxton technology. This allows the chip's clock frequency to be boosted when the instructions are not taking advantage of the processor's capacity.

The clock system has two frequency modes: fixed and variable. It starts in fixed mode and then is moved into variable mode by firmware. Configuration is via a translation table, which determines phase locked loop (pll), digital frequency dividers (dfd) and aligner divisors, along with fuse selected bus logic and core clock rates. Fuses determine the core start up and limit frequencies.

The variable frequency clock system features a pll which generates a multiple, M , of the system clock frequency, where M lies between 6 and 20. According to Intel's paper, pin selectable clock frequencies for Montecito are 200, 266, 333 and 400MHz. The multiplied clock is distributed to 14 dfds, where it is divided to the appropriate zone frequency. Each dfd, which features a delay locked loop (dll) and a state machine, selects from 64 dll phases generated from the pll clock. This, says Intel, allows the dfd's output frequency to vary from F_{pll} to $0.504F_{pll}$ in increments of $0.0164F_{pll}$.

Each core has three dfds, with a further 1GHz dfd for Foxton control. Each of the six Front Side Bus stripes has its own dfd and a dfd looks after bus logic. Each dfd output clock is distributed to second level clock buffers (slcb) for delay tuning to a resolution of 1ps. Each core also has 35 regional active deskew phase comparators to deskew neighbouring slcbs. Finally, slcb clocks are distributed to 7536 clock vernier devices (cvd) per core for local delay fine tuning. The result, says Intel, is less than 10ps of clock skew across the 21.5 x 27.7mm chip.

In tests, Intel has run the clock system at up to 2.5GHz from a 1.2V supply, in the process booting Linux, HPUX and Windows and turning on Foxton. 