



# Power point

**D**emand for battery powered devices with higher functionality, higher performance and lower power consumption means SoC designers are struggling to resolve conflicting constraints.

A common strategy for reducing power is to reduce supply voltage. But this can lead to lower noise margins and a potential increase in sensitivity to such problems as crosstalk. Meanwhile, higher performance means higher clock rates, which not only increase dynamic power, but also parasitic effects. Further, greater density and smaller process geometries bring more leakage current, which means continued power dissipation even when a circuit is idle. But, for a typical cmos SoC, dynamic power dissipation is the prime consumer of power.

The problem is compounded in that a combination of power related effects can result in voltage drop and signal integrity problems, impacting circuit timing and device function. For example, the impact of voltage drop is difficult to predict and

New eda tools for power analysis should help to optimise SoCs for low power operation and improve design efficiency. By **Louise Joselyn**.

may not be limited to setup timing violations. Also, the interaction of voltage drop and signal integrity effects is too complex to be diagnosed with traditional timing analysis tools. The end result can be a device failure, which may even be wrongly attributed to a yield problem.

To date, engineers faced with timing problems might have widened the timing and layout margins. But at smaller geometries across a large and complex circuit, this is inefficient as problems are only likely under certain conditions. Increased timing margins can lead to higher clock rates and larger clock buffers, yielding even higher power consumption.

To some extent,

there are circuit design techniques which can deal with – or at least minimise – the impact of dynamic power, such as clock gating, power down modes and optimising gate and interconnect delays. There are design and process techniques to control leakage current too, with low leakage processes under development.

SoC and asic designers have, for some time, bemoaned the fact that good eda tools to tackle power analysis and predict power characteristics accurately have not been available. It seems eda vendors are finally responding.

Power analysis tools that are becoming available range from relatively low cost point tools – claimed to provide fast and effective results within an existing tool flow – to multiple function interactive subsets of tools

combining detailed and accurate power and signal integrity analysis.

Not surprisingly, companies such as Cadence, Magma and Synopsys, have offerings in the latter camp and all have recently announced new products. Cadence and Synopsys admit their traditional analysis tools are no longer thorough enough for full chip sign off. Both believe only a new combination of interactive tools will provide the performance required at smaller geometries and that users can no longer rely on tools that employ approximations, simple load models or a single overall derating factor for supply voltage.

Cadence recommends the use of accurate parasitic extraction, advanced models



and simultaneous analysis of the effects of IR drop and signal integrity on timing before tape out. It has announced an integrated subset of tools comprising Fire & Ice QX, for detailed parasitic extraction, and VoltageStorm, for power rail analysis. The outputs of both feed the CeltIC NDC delay calculation engine. Detailed and accurate models are critical, Cadence advises, and it promotes the use of effective current source models (ecsms).

Another important issue, says Cadence, is the correct combination of static and dynamic analysis. Static analysis identifies gross violations and ensures the general robustness of the power rail. Dynamic

the package. Designers then use PrimeRail for vector based or vector free power rail analysis. For vector free mode, a Prime-Time kernel looks at peak power analysis based on the ic's switching activity, which PrimeRail uses for dynamic rail analysis.

Synopsys is working on integrating these tools with other software used in the design flow, including its IC Compiler and the JupiterXT floorplanner.

Magma's focus, meanwhile, is on an rtl to GDSII reference flow for low power designs. Key capabilities of its Blast Power and Blast Rail NX products, combined with its ic implementation products, include transient analysis,

36% on dynamic power.

The group also employed synthesis clock gating for 85% of the registers in the design, which turned off gates not in use. To reduce leakage power, the team programmed Cadence's RTL Compiler to leave critically fast cells alone, but to identify slower, less critical, nets and to swap them for low Vt cells.

Eda start ups are also targeting low power design with more application specific tools. Golden Gate Technology, for example, has just launched Power Optimize Gold and Power Plan Gold, which work with existing place and route flows from Cadence, Magma and Synopsys.

The first is claimed to reduce leakage and switching power, whilst meeting timing, signal integrity and electromigration constraints. It reduces power at dif-

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analysis helps optimise the number and placement of decoupling capacitors necessary to eliminate glitches. Unnecessary decoupling capacitors will only increase leakage current and overall power consumption, the company explains.

Synopsys concurs and has recently launched PrimeRail, a hybrid static and dynamic timing analysis engine which includes: an rlc (resistance, inductance and current) extraction engine from Star-RCXT; a kernel PrimeTime static timer for peak power or 'vector free analysis'; HSpice, for characterising standard cell libraries; and NanoSim, for modelling memories.

For power network sign off analysis, standard cell libraries and memory blocks are precharacterised before running either rc or rlc on chip extraction and rlc extraction on

decoupling capacitor insertion, automatic voltage island implementation, clock gating and power gating.

The flow can be tailored to specific foundry processes and ARM Artisan Metro low power libraries are used for flow development. Magma's latest news is collaborative support for the IBM/Chartered 90nm dual source platform.

A more extensive collaboration announced last year was the Silicon Design Chain Initiative, an r&d alliance between Cadence, ARM, Applied Materials and TSMC. Looking to tackle tougher SoC design problems, the initiative has developed a methodology targeted at reducing power. Dynamic power and leakage problems were tackled using multiple supply voltage techniques, in which voltage is scaled down for non critical blocks. On test chips, this saved

different stages in the physical design flow, working with placement and clock tree synthesis to reduce power consumption in the critical clock network.

Power Plan Gold creates architectural multivoltage island designs by creating complex power grids automatically. Working with silicon virtual prototyping tools, this gives designers accurate power consumption information earlier in the design flow, avoiding downstream iterations caused by undersized power grids, and wasted power and silicon resources caused by over designed power architectures.

Bringing power analysis into the virtual prototyping phase, Silicon Dimensions has announced a new version of Chip2Nite, a design planning tool aimed at logic designers.

In addition to power density analysis, Chip2Nite adds an ability to generate custom wire load models and a 'predictive' floor plan that does not require manual pin assignment. The tool outputs a thermal map pinpointing density problems, along with a report on every instance in the design and its power consumption. This information is then passed to the physical design team, which may decide to beef up its power mesh in critical areas. 

