



# Countering complexity

How are eda companies responding to the need to design high pin count packages onto pcs?

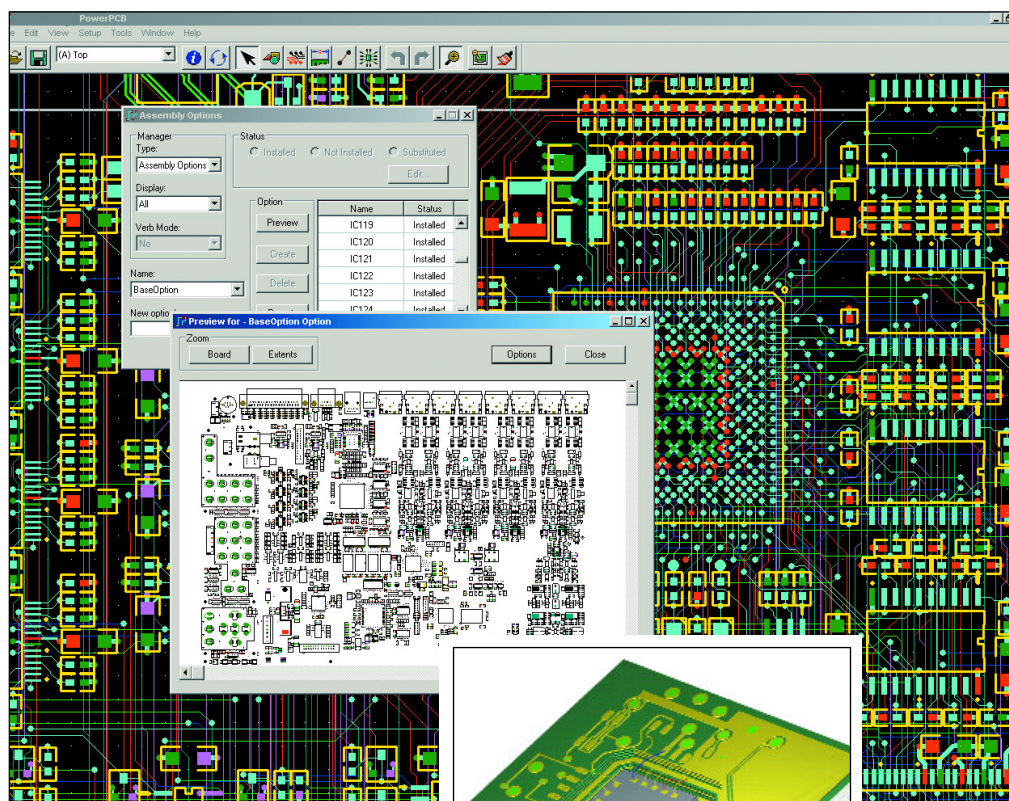
By Louise Joselyn.

High pin count packages are becoming increasingly popular. No longer reserved exclusively for specialist parts, commodity devices – including multichip memories and fpgas – are available in 1500pin bgas and 3000pin bgas are not uncommon.

Technologies such as system in package (SiP) are also gaining ground. Philips, for example, offers highly complex devices containing multiple die. SiPs have also found favour for devices requiring sensors combined with digital cmos circuitry and are finding application in the automotive and security markets.

From one perspective, these highly integrated devices can reduce board level design complexity, as interconnection between the rf and digital sections, for example, is achieved inside the chip. But there are still problems to solve when placing high density devices on boards. As a result, new board fabrication techniques, such as fine line HDI and multilayers with micro vias, are emerging.

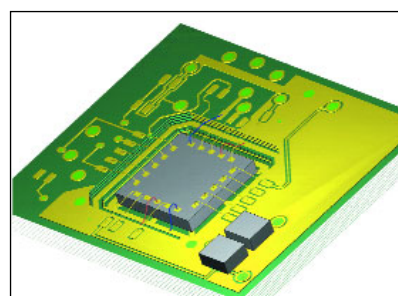
Whether or not such techniques are adopted, signal integrity remains a primary concern at board level. The potential for interference between devices on a chip requires careful consideration and analysis. Poorly designed or attributed pin outs can cause major headaches, incurring unnecessary delays and costs. A detailed understanding is required of pin assignment at the chip level and its effect on board level design, especially for rout-



ing related timing performance. Poor interaction can result either in errors in the fpga or a board respin.

Fortunately, there is increased activity amongst eda vendors and device manufacturers to alleviate some of the problems. Device vendors are not underestimating the systems level issues involved at board level. The key, they say, is to take a wider view – from silicon to system backplane – of the transmission line environment. And this is true for all complex devices, whatever their package style.

The answer, eda vendors maintain, is co design. This is the only efficient way of optimising both the chip and the board design, particularly in terms of performance and minimising signal integrity problems. Truly concurrent co



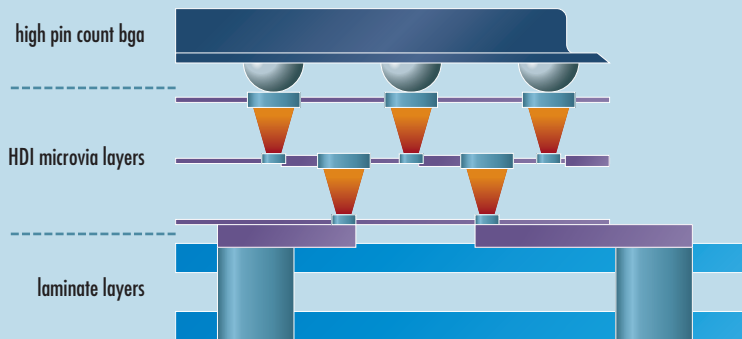
Zuken offers both package and pcb design within its CR5000 suite.

design allows the chip designer to lock certain pins whilst leaving others for the board designer to allocate, avoiding potentially catastrophic pin swaps. Timely analysis allows both chip and board designer to make adjustments during the design process, rather than having to rework it afterwards.

For fpgas, co design tools seem well established, with companies including Cadence and Mentor Graphics supporting this methodology. For other devices,



**Figure 1: High density interconnect**



## An FPGA opportunity

Altera and Xilinx both recognise that signal integrity problems are having a significant and not easily predictable impact on board design. The issues are especially important in devices with fast edge rates and wide databuses.

The problem, says Xilinx, is that simultaneous switching output noise grows in severity and there are two contributing factors. First is noise due to via field crosstalk, which can manifest itself at the package and/or board level. The problem is exacerbated when multiple I/Os in the region switch simultaneously. The second factor is compromised power integrity due to high package inductance. Again, parasitic package inductance can

lead to ground bounce or  $V_{cc}$  bounce at board level.

Citing that good package design is critical to good noise performance in fpgas, Xilinx offers its SparseChevron package claimed to provide the optimal pinout architecture for the best distribution of ground/power and signal pins. Further, with every signal pin adjacent to a return pin, the package provides a low impedance path for the return currents.

Altera offers specific design advice and guidance. It specifically recommends engineers ask for packaging information relating to signal integrity characterisation results, such as correlated I/O buffer and package model data. Further, the firm suggests, determine whether signal integrity was an issue when the fpga was designed. An obvious tip, maybe, but often overlooked.

solutions are less evident, but more generic tools under development should help designers optimise chip level I/O and board design concurrently.

One critical issue is obtaining good 2d and 3d device models. "Gone are the days when the system designer could take a data sheet and create a model for pin outs," said John Isaacs, director of market development with Mentor Graphics. Further, there seem to be no commonly used standards to ensure a consistent requirement or format. Not all device vendors are prepared to provide the detailed information on packaging that customers require.

There is an increasingly urgent requirement for design tools that can model and simulate accurately for signal integrity and emi. Signal integrity tools have been offered by eda vendors for some time. Some are highly accurate, require detailed models, can take a while to generate the results, work in isolation and require an iterative approach to design. Others are designed to provide an approximate simulation, but can be used at various points during the design process.

For SiPs and stacked or multilayer packages incorporating wire bonding, there is, literally, an extra dimension and

3d analysis is necessary, with subsequent impedance calculations. A number of dedicated point tools are emerging to tackle this from firms such as Ansoft.

In terms of general eda tool support, Zuken combines both package design and pcb design in the same suite – CR5000. This, the company claims, makes it a fairly simple matter to align package pin outs and board pin outs to provide more optimal routing, with fewer crossover routes and fewer layers. Further, the tool uses gridless autorouting to route out of the package (which may be wirebonded) to the board itself. Recently, Zuken has added a rules based 3d checker for verifying the routing in the z dimension for wire bonded devices.

Cadence supports a codesign methodology with its Allegro system interconnect design platform, which, it claims, is easily integrated with its Package Design and Package SI tools. Mentor, meanwhile, takes a similar line, incorporating modules for advanced packaging design within the pcb design software and ensuring a common database is supported throughout the design flow. This allows the designer to capture the die and I/O data required to create the necessary models for analysis at the board level.

But while co design appears to be the most logical methodology for handling high density, high speed devices in advanced packages, the emerging tools may not yet provide the entire solution.

Rene Penning de Vries, cto of Philips Semiconductors, stated recently that SiP eda tools do not yet exist. He added they will need to simulate not only the electrical aspects of the circuit, but also the thermal and mechanical sides. Whether such tools emerge independently or evolve from pcb design software, they would need to work in a common design environment.

For a large section of the design community, however, the supply/demand gap is not what tools can be provided, but what tools can be afforded. Isaacs made a final comment: "Customers need to understand the leverage to be gained in using not only the latest device technology, but also the tools that can best optimise that design, in terms of performance and cost." 