



Analogue outdoes digital

Signal processing the analogue way. By Roy Rubenstein.

Digital may get much of the attention but, for certain signal processing tasks, analogue has virtues that are unmatched. Speed, compact layouts and extreme low power can all be achieved on an analogue design implemented in a deep sub micron process.

“We designed an analogue 90° audio phase shifter – a Hilbert Transformer,” says Professor Peter Saul, partner and cofounder of Saul Research. “Just after that, an article appeared describing a dsp version. The [dsp] spec was marginally better, but the power consumption was 1000 times greater.”

Saul Research is a family firm that happens to be a fabless design house. Its services range from feasibility studies to delivered prototype analogue signal processing (asp) ics. “Most of our customers come along with a question as to whether their chip can be made at all, or economically,” says Saul. “We start with the customer’s idea, then turn it into a prototype.”

ASP refers to complex circuits where the signal passes through several analogue stages. Just as with dsp, the signal is transformed or characterised. For asp, signal filtering is common while other

tasks include complex manipulations such as phase shifting as well as log and antilog conversions.

Applications using asp tend to be low power, low noise. “We do lots of circuits for radio – handhelds and radio links between equipment,” says Prof Saul. Sensors are another; for example, circuits that measure capacitance changes due to MEMS movement. “Such applications are for battery powered, portable equipment put in the field and left for months.”

Fab choices

For a company undertaking an asp ic design, choice of foundry is a key decision. Even getting fab access can be an issue if the design run involves prototype numbers only. Another issue is selecting the right process, given the wide choice.

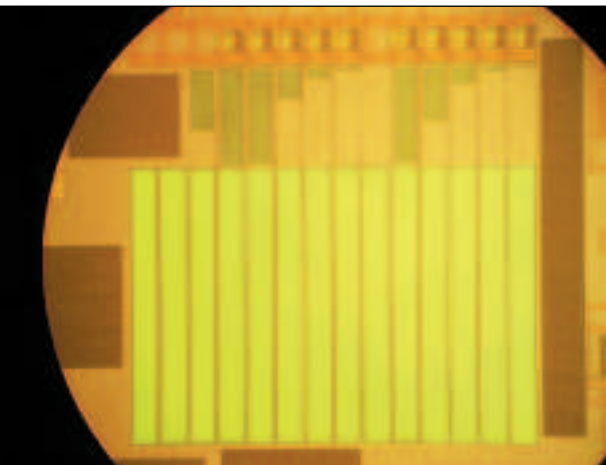
Europe has three main cmos foundries: austriamicrosystems; X-Fab; and AMIS. There are also specialist firms such as Zarlink offering a bipolar process, and IHP for silicon germanium. Saul Research has designed products using several foundries. “As a small business, we have to have access to a foundry’s design data without being able to promise a very large order,” he says.

This can be an issue with foundries wanting to see 100 or more wafer starts a year – equivalent to 300,000 analogue chips,

A way around the problem is multi project wafers (MPW), where companies split the cost of a production run – and the resulting volumes – by placing their designs on one wafer. Saul Research has used MPW provider Europractice extensively. “It has been an enormous help. I think we are its biggest UK industrial user when measured by numbers of designs placed, and about third overall,” says Prof Saul. “We also use more varied processes than anyone else.”

Foundries offer cmos processes with feature sizes ranging from 0.7µm to 90nm. For digital, smaller mostly means better, but for analogue, voltage headroom becomes an issue with process shrink.

The rule of thumb regarding the safe limit is 10V per micron of minimum process dimension. “A 0.35µm process is good for 3.5V, usually translated as 3.3V, while 0.18µm is only good for a 1.8V supply,” says Prof Saul. Whilst logic circuits can operate close to the voltage rails, analogue circuits need enough voltage to operate a differential



Although Saul Research's analogue 90° audio phase shifter has slightly less performance than a digital equivalent, its power consumption is 1000 times less.

pair or current tail. "That means the voltage swing is around 1.4V [for a 0.18µm process] – not much for some applications," he says.

Circuits can be designed using a smaller voltage swing, but performance is compromised. "We are designing 3.3V devices in the 0.35µm regions of a 0.18µm process," says Prof Saul. "This gives us 3.3V supply, 0.18µm process compatibility and, surprisingly, better all round performance than we would get with either."

The designer's preferred approach also affects process choice. Prof Saul

favours analogue designs that use resistors and capacitors. "We have put down many hundreds of megohms on some chips; single resistors of 200Mohm are no problem on the right processes and have been highly reproducible."

The alternative approach avoids passives, using FETs instead. This allows designers to embrace leading edge process dimensions. "At least one or two process generations ahead of us," says Prof Saul. But the approach brings design risks. One is supply voltage rejection – greater power supply ripple can appear at the circuit's output; another is component value variation. "All FET designs really only make sense for the in house design groups," he says.

Nano converter

Prof Saul cites the company's recent 8bit d/a converter design for QinetiQ to illustrate asp design issues. "The idea was to use well known digital cells, yet its output is clearly analogue," he says. The converter was a proof of concept design to show that a 0.35µm process could deliver extremely low power consumption and a sub mV bit size. The design involved adding an analogue switch to the converter's resistor chain. "It just needed some transmission gates – similar to 4x inverters – and resistors to be added to the digital components," says Prof Saul.

Another aspect was ensuring the

resistors matched well, such that value errors averaged out overall. Once the cell was crafted, 256 were laid out to form the 8bit design,

The result is a small area, 100mV d/a converter – equating to 0.4mV per bit – with a standby current of 100nA. "No one thought a 1mV per bit d/a converter was possible," says Prof Saul. The converter, which has a tiny power consumption, gives a dc output without taking current. Given the 2.5V reference voltage, that equates to 250nW.

As for Saul's Hilbert Transformer circuit, it is a purer asp example. The circuit was developed for a single sideband generator and receiver circuit. One application is for direct conversion of an rf signal. Another use is for a medical design. "The company had a medical device and wanted to develop a handheld version, hence the requirement for low power," says Prof Saul. The chip takes 120µA at 3.3V.

Prof Saul believes the use of digital cells as analogue building blocks will be an area that designers will increasingly explore. "An inverter makes a fine broadband, high gain amplifier if the dc conditions are right – and that might take only one resistor," he says.

Similarly, rf switches can be formed from minimally changed logic gates. For example, a 4x gate can give good enough performance for some applications, while using very small chip area, and rapid layout. "Layout time is always an issue with analogue; there are few standard circuit blocks available," he says.

A further analogue cmos design issue is interfaces. "With the right process, 50V or more is possible, or currents of say 0.5A," says Prof Saul. These need careful design to stay within the foundry design rules, but it can be done.

Meanwhile, asp opportunities will continue to be the centre of low voltage designs as cmos processes shrink, he says. This will include signal conditioning, such as low noise amplifiers and filtering in the analogue domain, as well as decision circuitry. "We are talking low noise, low power designs," Prof Saul concludes, "down to the nanoamps." 