



After months of developing your latest design using the best tools at your disposal, it's reality time. The prototype has arrived and is ready for testing. All your careful development work, rigid design rules, signal integrity analysis and presimulation passes will ensure the prototype will work to specification with little chance of needing design revisions – what's more, it even looks great!

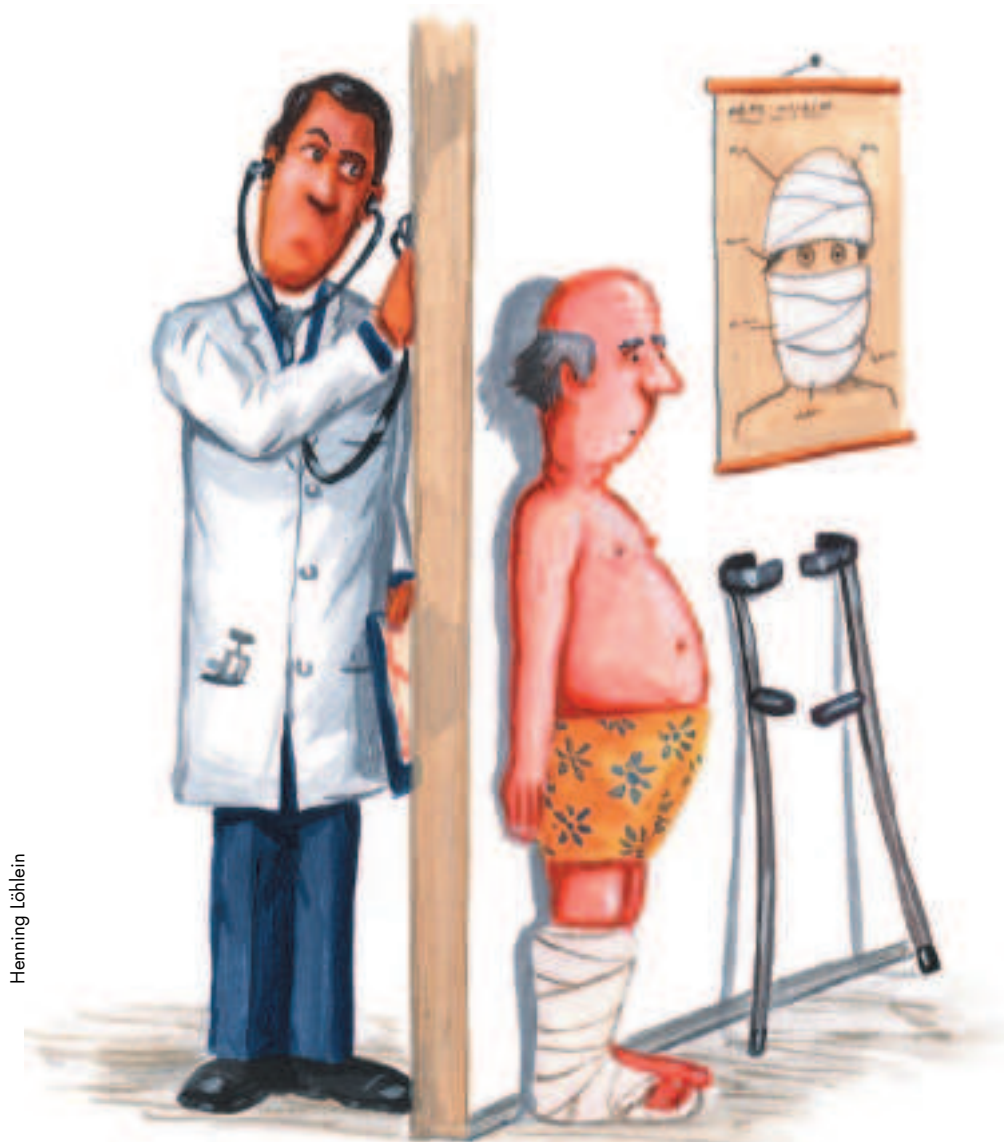
But when you power it up, a major section doesn't work as expected. The next step is probably cursing, followed by a process of diagnosing and correcting the problem. That will generally involve a gaggle of test instruments linked to flying probes. This, coupled with the design documentation and your troubleshooting skills, allows you to trace signals around the populated board to deduce the culprit.

Unfortunately, dense multilayer boards and the latest component packages, such as bgas, has made this much harder. With traditional testing and debugging techniques relying on physical access to key points and device pins, this approach is often unworkable or, at best, inadequate. Indeed, where bgas are the main elements, inaccessible pins make effective board diagnosis close to impossible. Like a doctor attempting to diagnose a patient locked in another room, an engineer can extract little tangible information.

Then there's an added complication for development engineers resolving prototype errors. Unlike the process of fault finding a unit that has developed a component or track level fault, a prototype may also be crippled by a source design error, a board assembly problem or a board level manufacturing fault. The design has never worked, so that frame of reference does not exist.

One solution to gain the required verification and debugging access is to include a large number of test points in your prototype board design, exposing the key points and signal lines. Unfortunately, in larger complex designs, this approach can have a significant impact on the board development time and its cost, complexity and size may not justify the insurance of being able to access the prototype's internals for troubleshooting purposes.

What's up Doc?



Henning Löhlein

How to ease the board level diagnosis problem. By **Rob Evans**.

In response to disappearing pin access and the increasing density of new device packaging, the Joint Test Action Group (Jtag) was formed in the late 1980s to address these restrictions. This work culminated in the Boundary Scan methodology (IEEE1149.1) introduced in the

early 1990s. Boundary Scan compliant devices include additional circuitry to create an embedded serial communication bus that can be programmed to capture, then transmit, snapshots of the logic state of all pins. Using a four wire serial bus, all compliant devices can be chained



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Rob Evans, **Altium**

in the board layout to facilitate final testing and debugging via a suitable interface.

The potential therefore exists to troubleshoot and verify complex designs that use pin inaccessible high density devices through simple software interrogation. In turn, the proliferation of boundary scan compliant devices opens this cost effective possibility to all new designs – and, in particular, those based on devices such as fpgas – without the need to rely on physical probing and external stimulation.

Given a high level of boundary scan support within a design, logical fault finding techniques can be used to eliminate possibilities, then track down the problem – be it a dry solder joint, shorted track, incorrectly orientated component or, heaven forbid, a design error.

Faced with a range of electrical or functional fault possibilities, boundary scan analysis can decrease design verification and testing time by helping you eliminate possible causes, whilst guiding you to the source of the prob-

lem. Even better, if that capability was an integral part of the product development system, working with a prototype would no longer be a disconnected and cumbersome step in the process of taking a design from concept to completion.

Real time action

Altium Designer provides native support for this approach through a range of boundary scan enabled features that can communicate in real time with suitably equipped boards. This might be through Altium's fpga prototyping board – the NanoBoard – or any boundary scan enabled board via Altium's Universal JTAG cable or through expansion connectors on the NanoBoard itself.

Once connected to the boundary scan interface, Altium Designer can access the boundary scan devices on your prototype board, then display the pin state results live on your pc. Any Jtag compliant device can be accessed by including the Boundary Scan Description Language file supplied by the device vendor. This provides a complete Jtag based insight in the internal state of your prototype.

How you choose to display this information will depend on your preferences or the type of pin state information that will most help you. Altium Designer offers design document level access to pin states through schematic based test probes that are simply dropped on to the circuit where the logic state of a Jtag accessible line or bus is displayed in real time.


If your preference or area of concern is at a board layout document level, Altium Designer also features real time pin state monitoring at a device and connected track level. This is ideal if you suspect that a misplaced component or faulty solder joint is preventing signal

transfer between the pins of a device – or devices – where connected tracks are highlighted in real time to represent their logic state.

Beyond point monitoring at a document level, Altium Designer also features an enhanced boundary scan device viewer window, capable of displaying the state of all pins of a device in real time. This live view of a selected boundary scan device presents a continuous tabular update of all pin states, plus a representation of the pin action on a matching device schematic symbol and pcb footprint. When diagnosing or verifying the operation of your prototype, Altium Designer's real time viewer delivers live information that provides a probeless view of the board's internal signals.

Interacting in real time

While a standard boundary scan chain is ideal for accessing the state of compliant devices and connections on a board assembly, it can also be adapted to higher level uses, such as an in circuit programming port for fpgas and other programmable devices. Taking this to the next level, another working group has developed the Nexus standard that harnesses the existing boundary scan 'hard chain' to create a 'soft' chain that facilitates working with embedded microprocessors – access to logic states then includes the programmed soft devices within an fpga's fabric.

Altium Designer leverages the Nexus standard by providing native level communication with the embedded structure programmed in an fpga, enabling an interactive way of developing electronic products. LiveDesign and Altium Designer form a unified design system that allows you to interact in real time with reconfigurable hardware implemented on an fpga platform using on screen virtual test instruments and processor debuggers – plus, of course, the document and window based pin state monitoring enabled by the hard boundary scan chain. 

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