

Push me, pull you

SoC and standard products are creating conflicting requirements for analogue processes.

By **Paul Dempsey**.

For some time, 0.18µm cmos has been considered the 'sweet spot' for the implementation of a/d conversion. The node offers high performance transistors, the mosfets meet the requirements of high resolution applications and a 1.8V power supply has allowed designers to reuse architectures and other techniques that boast a couple of decades of maturity.

However, at next month's International Solid State Circuits Conference (ISSCC) in San Francisco, more than half the papers on a/d converters are for implementations at 90nm and smaller. So, is the analogue world gearing up for a major node shift?

The answer is both 'yes' and 'no'. Whilst the 90nm trend runs across both the Nyquist and sigma-delta a/d worlds – and the ISSCC papers are more than 'science projects' – the trend is both market driven and market limited. Right now, this is mostly about system on chip.

"We are not so much focusing on standalone functionality as SoC. It's been the situation for years that analogue does not dictate which node is used. As analogue and mixed signal designers, we have to follow digital," says Leo Warmerdam, a senior director of NXP Semiconductors' research arm.

NXP is presenting three of the deep submicron implementations at ISSCC (including one in 65nm), and, not surprisingly, is joined in the 'envelope busting' by other SoC specialists – commercial and academic – such as Fujitsu, LG Elec-

tronics, IMEC and UCLA.

All acknowledge that, today, 90nm is more a necessity than analogue wide desirable, because it certainly is not easy. "It is extremely challenging," says Warmerdam. "And as you make the migration from one node to another, the cost of a digital function decreases and the cost of an analogue function increases."

For those whose business is more geared towards standalone a/d converters, these challenges are perhaps – and with the caveat of 'for now' – just too much.

"There are a good few markets, like cellphones or laptops, that are large enough to recoup the NRE [for the a/d as part of a 90nm SoC], but would you do this for a standard product?" asks Dave Robertson, product line director in the high speed signal processing group at Analog Devices and chair of one of ISSCC's data converter subcommittees.

"If you're selling components in thou-

sand piece quantities, it takes a lot of those per year to pay for your [90nm] seven figure mask set – and that's if you get it right first time."

Bob Dobkin, cto and founder of Lin-



Bob Dobkin: "Foundries aren't encouraging process migration."

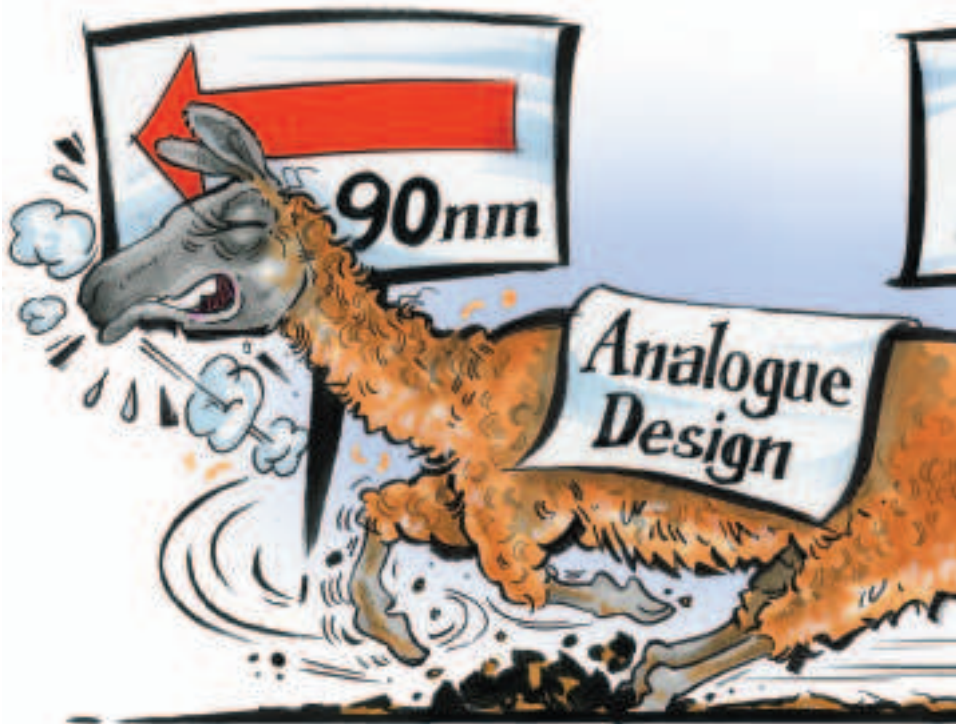


Illustration: Don Seed



Rudy Lauwereins: "One of the advantages of 90nm is you have more logic available."

ear Technologies, agrees. "If you have to go as fast as possible, then you're at 90nm. If you have an SoC, then you're at 90nm. But if you are going to make a standalone a/d with high accuracy, then 'no'. The cost of 90nm just doesn't work if you're looking at a couple of hundred thousand units total on the part."

Nevertheless, the 90nm work to date is highlighting a number of obstacles that face any broader analogue transition. There are obvious issues over power sup-



ply and accuracy, and the likelihood that long favoured architectures will require serious revision or substitution. There are concerns over the available dynamic range. But, in terms of process technology, one increasingly familiar concern stands out – the impact of all those lithographic tricks needed at 90nm and smaller.

"When you go to scaled down technologies, then variability increases and this is a problem for analogue, because you often need matched components. The sensitivity is far, far greater," notes Rudy Lauwereins, vice president Design Technology for Integrated Information and Communication Systems at Belgian research institute IMEC.

Some of this can be avoided by replacing analogue components with digital controls. "One of the advantages of 90nm and smaller is that you have so much more logic available. You can start to do these kinds of replacement efficiently where they would not have worked at even 130nm – and so you know these techniques will get more efficient as you go to smaller nodes. You also start to have more options for redundancy," says Lauwereins.

IMEC and the other presenters will outline how far it has been able to go down this road at ISSCC – but still the variability problem will not entirely go away.

"I dare say we're one of the pioneers in the usage of these digital control functions. We know how to play that game fairly well and we know that, as we progress to newer cmos technologies, we can get still better functionality out of it," says Warmerdam.

"But it's still the case that, for an analogue and mixed signal designer, everything is determined by the quality of the models. If those are correct, the engineer can do a near perfect job."

Right now, however, in an era of heavy post processing – driven by the design for manufacture requirements of 90nm – there is still a big question mark here. The models change 'all the time', says Warmerdam. A loss of WYSIWYG security or gaps in knowledge hurts AMS engineers just about more than anyone else.

Rodney Chandler, a research student at UCLA and co author of one of its

ISSCC papers, notes: "We had a design kit from the foundry, but there were big holes in the design flow. For example, getting timing verification was a real pain. That's just one example where getting the analogue and digital flows more integrated would help. And there are others."

To some extent, it is accepted that this will happen in the analogue world. "The learning curve on each technology causes what we call the mixed signal lag," says Robertson. "The digital guys get the tools on a new technology and then, nine to 18 months later, the mixed signal products become available."

"And the other irony," says Dobkin, "is that foundries aren't encouraging migration. They still have a lot of capacity at 0.35µm and you're hearing about it



Dave Robertson: "The learning curve on each node causes what we call the mixed signal lag."

at 0.25µm and so on. The foundries are looking at how they can best fill that capacity, where the higher voltage devices are that they can easily make on those lines. That's their priority for analogue, so there's an obvious support question. We'll move when we need the speed, but we aren't at that point yet."

And, since he has been to 90nm, Chandler perhaps sums up the situation best. "The cost and pain of 90nm mean that, unless you need to integrate all these things because of SoC, or low power demands or pcb real estate, there are good reasons today for staying at the existing, popular process nodes." 