If the **CAP** fits . . .

Customisable microprocessor offers asic costs, but lower risk. By **Tim Kubitschek**.

Today's system designers face many challenges. Designs are becoming more complex incorporating, for example, 32bit risc microprocessors, 256kbyte of sram, DDR2 memory and so on. That complexity brings greater risk of design iterations and delays during the product development phase that can lead to missing market windows and impacting profitability.

Given these trends, many companies have mandated that designs should be implemented using standard products wherever possible to mitigate risk. Standard products minimise the design risk, since they are available off the shelf. However, there are drawbacks. Standard products do not allow customisation and, as there is no way to build company secrets into a standard product, designers need some means to provide custom features.

FPGAs are one approach; they have low upfront costs, but require RTL logic design, synthesis and verification. Verification can be onerous, with numerous detailed test benches required to validate all test cases.

Another option is an asic. Standard cell asics offer highly customised, very low unit cost solutions, but have high upfront development costs – more than $1million for a 90nm design with sophisticated IP content – and development time can be 12 months or more for a complex design.

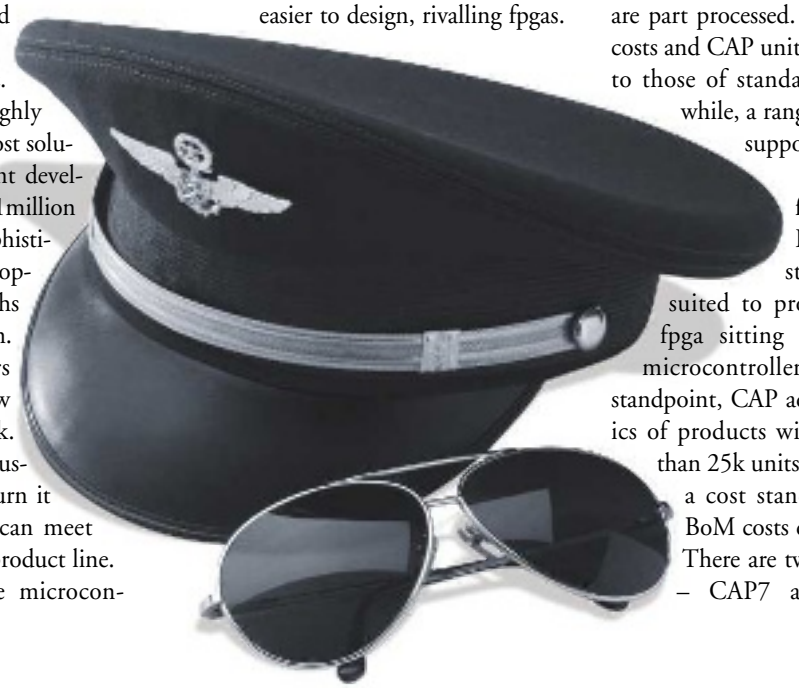
It is clear that designers want a solution that has low upfront costs and low risk. They want the ability to customise the design and to turn it quickly. Atmel believes it can meet these needs with the CAP product line.

CAP is a customisable microcontroller platform – a microprocessor based solution with fast local memory, a wide range of peripherals and a metal programmable (MP) block, which allows custom IP to be added.

Low risk, but customisable

CAP can be thought of as the integration of a low risk standard product micro with customisable logic to produce a single chip device with a unit cost comparable to that of a standard cell asic.

CAP is enabled by Atmel's Metal Programmable Cell Fabric (MPCF). With nearly identical routed gate densities to those of standard cells in the same process, the technology makes CAP cost competitive with standard cell asics and easier to design, rivalling fpgas.



The custom designed MPCF library contains more 400 cells. It has an eight transistor core cell measuring 3.2 x 2µm and uses two metal layers for interconnect.

Because CAP is based on standard cell asic technology, it offers higher performance, lower power consumption and a lower unit price when compared to a microcontroller in combination with an fpga.

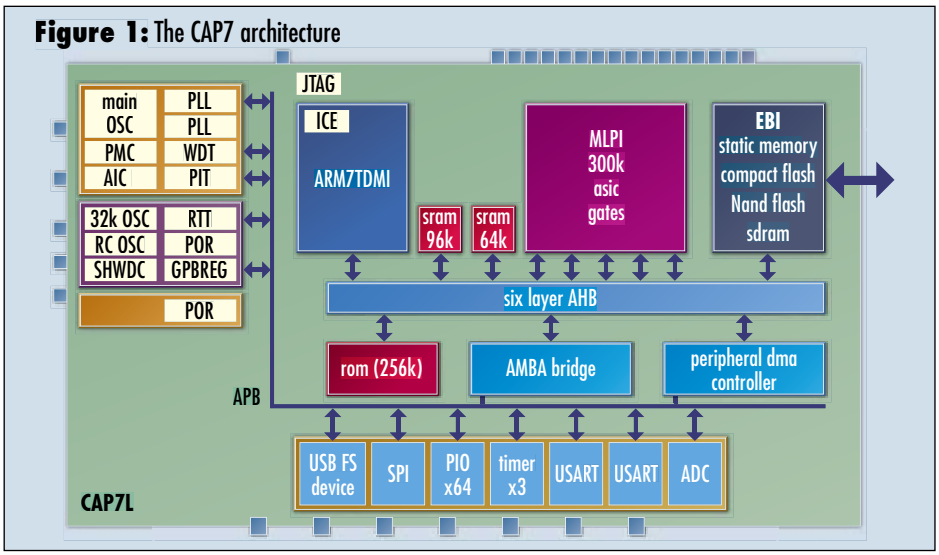
The first CAP products are ARM based, with the core, local memory, the internal bus interface and peripherals already designed, laid out and verified in silicon.

There are a number of advantages with this approach. Risk is reduced since the ARM IP is fully verified in silicon. Development time has been reduced, since the designer only has to focus on the portion of logic that would typically be in an fpga. Design turnaround times of less than six months are achievable and fabrication time is reduced since wafers are part processed. Designers save NRE costs and CAP unit costs are comparable to those of standard cell asics. Meanwhile, a range of design tools and support is available.

So where does CAP fit in the market? From a functionality standpoint, CAP is suited to products that have an fpga sitting alongside an ARM microcontroller. From a volume standpoint, CAP addresses the economics of products with volumes of more than 25k units per year whilst, from a cost standpoint, CAP lowers BoM costs dramatically.

There are two CAP architectures – CAP7 and CAP9 – both

Figure 1: The CAP7 architecture



designed to cover a broad range of ARM based applications.

The first CAP products are the AT91CAP7S, based on the ARM7TDMI processor core, and AT91CAP9S, based on the ARM926EJ-S. The AT91CAP7S has 160k of on chip sram and a 450k asic gate MP Block. Some ARM peripherals are instantiated in the fixed portion of the design to address low cost applications. Additionally, other peripherals can be designed in the MP block.

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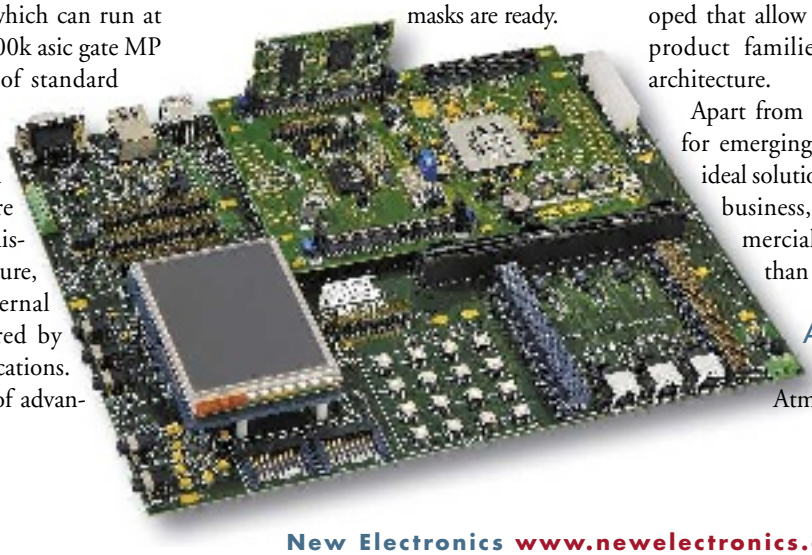
The AT91CAP9S, which can run at up to 200MHz, has a 500k asic gate MP Block and a number of standard interfaces and high performance peripherals. These are connected via a parallel bus structure that, together with a distributed DMA architecture, delivers the high internal data bandwidth required by deeply embedded applications.

CAP has a number of advantages over standard cell asics, including lower design costs since the predefined IP blocks – including ARM processor, memory, analogue and I/O – have been designed and verified in silicon. With the timing analysis, clock tree generation, Jtag, BIST and scan logic already implemented for the fixed portion of CAP devices, design time is reduced. Design NREs are also reduced, since only metal masks must be generated – the lower layer masks are unchanged and reused.

Less time, less NRE

An important point is that there are two components to development cost savings when using CAP. One is less engineering time, the other is the lower NRE to implement the design in silicon.

Another advantage of CAP compared to standard cell asic is that fab processing time is halved, since wafers are staged prior to metal and completed when the metal masks are ready.



CAP offers performance and unit costs comparable to those of standard cell asics, but at a fraction of the overall cost.

Perhaps the most important benefit is unit cost. Integrating fpga logic within the MP block replaces the fpga at a fraction of the cost (less than 20% of the cost of an fpga, depending upon the size of the device it replaces). The reason is gate density; the MP Block's gate density is comparable to that of a standard cell asic (210k gate/mm≈), more than 20 times that of an fpga (10k gates/mm≈).

CAP can also support five times the performance of fpga and can reduce power consumption by a factor of five.

CAP provides an alternative to placing an fpga alongside an ARM standard product and is suitable for volumes in excess of 25k a year.

Atmel will be introducing a family of devices to provide flexibility in the development of CAP based end products. That flexibility will be provided with a number of options in predefined ARM peripherals, as well as a variety of MP Block sizes and on chip sram sizes. Future devices will expand to include flash memory and additional processor options, including ARM11 and AVR32.

In summary, CAP allows companies to take on a larger number of development projects, since the design resource for each product is reduced compared to that of a full custom standard cell asic. And, with more than 70% of the design already completed, CAP allows companies to lower risk. Product development time is accelerated and design costs are reduced. CAP devices enable sophisticated ARM based designs to be developed that allow companies to launch a product families based on the CAP architecture.

Apart from being an ideal solution for emerging businesses, CAP is an ideal solution for a medium volume business, offering a more commercially optimised solution than fpgas.

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