



Transceiver take up

Manufacturers are boosting the number and type of transceivers on their fpgas. By **Roy Rubenstein**.

Adding transceivers to fpgas is not new; it was first done a decade ago as part of the former Lucent Microelectronics Orca family. But it is now commonplace, especially with the emergence of several serial interface standards. “These [transceiver] fpgas account for 10 to 20% of the total market and this is growing fast,” said Shakeel Peera, director of strategic marketing, high performance fpgas for Lattice Semiconductor.

Altera launched its latest family of transceiver fpgas in May. Dubbed Arria GX, the family targets three specific serial interface standards: Gigabit Ethernet (GigE), PCI Express (PCIe) and Serial RapidIO. “Some applications are so cost sensitive that we believe a family like this will expand the market overall,” said Altera’s Danny Biran, senior vice president of product and corporate marketing.

Arria complements Altera’s Stratix II GX, a family of transceiver fpgas that supports six serial interface standards at speeds up to 6.375Gbit/s. Lattice has, for almost a year, had two transceiver fpga families – the SC and ECP2/M – that tar-

get different cost/performance points, whilst Xilinx’ Virtex 5 family has four platforms, three of which have on chip transceivers. “That’s because so many applications require it,” said John Heighton, Xilinx’s EMEA senior manager for product solutions marketing.

Altera decided to launch a lower cost fpga family focused on these three standards only at speeds up to 2.5Gbit/s. “Of the various interface flavours [supported by IIGX], these three are breaking away,” said Biran.

Support for GigE reflects its widespread adoption within telecom equipment. The transceiver is used to terminate traffic on copper or optical links, for backplanes and even between chips so the entire data path remains Ethernet. The interface’s use is spreading to industrial applications and markets such as broadcasting.

One Xilinx customer is using a Virtex 5 fpga for Video over IP. The fpga SoC takes either standard or high definition raw video, performs some digital signal processing before sending the video to

either the GigE or PCIe transceiver. “Such video over IP – with the dsp, PCI Express and gigabit Ethernet interfaces within the one fpga – is a growing opportunity,” says Heighton.

PCIe is the latest variant of the long standing PCI computer expansion card standard. It is adopted by Intel processors and PowerPC devices used for telecoms as part of the control plane. Unlike its predecessors, PCI Express Revision 1.1 uses serial links – or lanes – each capable of bidirectional communication at 2.5Gbit/s.

The PCIe lanes range from one (1x) up to 32 (32x), but Arria GX supports 1x and 4x. “PCIe is the interface of choice for the pc and server world,” said Biran. “It is now in high volume, the cost is going down and it is attractive for many applications.” Medical imaging is another market. For example, an fpga provides a PCIe link to a single board computer, whilst interfacing it to the sensing system such as ultrasound and the system memory.

The third serial standard is RapidIO, a packet switched based interface that also has a parallel implementation. Serial

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RapidIO supports one (1x) and four lanes (4x) at 1.25, 2.5 or 3.125Gbit/s. The Arria GX family targets the first two speeds only.

Serial RapidIO transceivers remain a niche market for fpgas compared to GigE and PCIe, but demand is growing as Serial RapidIO becomes adopted as part of ics, such as in TI's C64xx dsp family. Not surprisingly, Serial RapidIO is used for applications requiring fpga and dsp hardware. The dsps execute program code, whilst the fpgas are used as a coprocessor for computationally intensive tasks.

Having fpgas with Serial Rapid IO transceivers enables the fpgas to interface directly to the dsps. "Serial RapidIO is very good for peer to peer, switched communication," said Peera. "Anywhere you see dsps and fpgas and there is a need for distributed processing." Such examples include Wimax and 3G wireless basestations.

ASSPs and fpgas

Having three serial standards used across the telecom, datacom, industrial and broadcasting markets explains the growing prominence of transceiver fpgas. Vendors typically adopt the best ic for a

specific application, with the serial protocol being a secondary concern. FPGAs perform an important role as bridging devices, whilst challenging application specific standard products (assps).

"If the assp does exactly what you need, then it is the right solution," says Biran. But if the design requires more than a physical interface (PHY), then an fpga becomes the preferred solution. Biran cites industrial applications that use legacy protocols as one example. "The market isn't big enough to justify developing an assp due to the cost." An fpga can interface the legacy protocols to one of the newer interfaces.

"There are always going to be applications for which assps do not yet exist, where standards are still evolving or where the system company has unique value it can add through programming some of the on chip logic," says Jordan Selburn, an analyst at iSuppli.

Designers under time to market pressure are also turning to fpgas, argues Peera: "Can I take a specific function on a line card and implement it inside an fpga using the latest technology at a lower cost and lower power? More and more [designers] are saying 'yes.'" FPGA gate counts continue to grow, as do the non recurring

engineering costs of assps. "FPGAs provide an extra layer of customisation and a value add when you have three or four serial standards fighting it out," says Peera.

New fpgas

Altera's Arria GX family consists of five devices that range from 21,580 to 90,220 logic elements, up to 4.5Mbit memory and 176 18x18 multiplier accumulators (44 dsp blocks). The number of on chip transceivers ranges from 4 to 12. "These are mid range devices: less than 20,000 logic elements is very small, while Stratix II GX has up to 180,000," said Biran. "Arria is aimed at designers using an fpga for the first time, so we wanted a robust transceiver. We leveraged the II GX transceiver that is at 90nm."

In contrast, Xilinx's Virtex 5 is a more general fpga family, supporting additional interfaces to Arria's tailored three. These include Sonet/SDH for telecom, Fibre Channel and Infiniband datacom standard and video interfaces. It also supports PCIe (1x to 8x), Serial RapidIO, including the 3.125Gbit/s data rate, and GigE. It also supports 8 to 24 transceivers and is implemented in a 65nm process.

Lattice claims to be the first to tackle the transceiver fpga market with two families. The high end SC has transceivers for the serial standards, as well as others such as the stringent Sonet/SDH. It also includes support for parallel I/O and up to 32 transceivers. The ECP2/M, aimed at cost sensitive applications, uses more compact transceivers and cheaper programmable logic.

Meanwhile, since Altera announced the device in May, the supporting design software has been downloaded by users in several markets. "FPGAs, in general, are mainly used for datacom and telecom, but with Arria we are seeing a lot of interest from test and measurement, medical, industrial and office equipment markets," Biran concluded. ☺

